SEMICONDUCTORS, COMPOUND

1. Introduction

In the most general sense, the term compound semiconductor encompasses a large number of materials, most of which crystallize in either the zincblende (cubic), wurtzite (hexagonal), or rock salt (cubic) crystal structures. Examples of these structures are GaAs, GaN, and PbS, respectively. More exotic examples of zincblende semiconductors are $ZnSiP_2$ and Ga_2Se_3. The latter crystal is a defect zincblende structure in which one-third of the Ga sites are structural vacancies. Groups 13 and 15 (III–V) and (2, 12) and 16 (II–VI) compounds that crystallize in the zincblende structure are of significant value for electronic and photonic device applications. The III–V nitrides, AlN, GaN, and InN, crystallize in the wurtzite structure and are being developed for ultraviolet (uv), blue, and green light-emitting diodes (LEDs) and lasers and high temperature and high power electronics (1,2). Solid-state light sources are currently being developed from the Group 13 nitrides and phosphides that rival and even surpass incandescent and fluorescent light sources in energy efficiency. The Group (2, 12) and 14 (II–VI) compounds are of value primarily for photonic applications. Blue lasers have been created from ZnMgSSe alloy heterostructures (2,3). CdSe, ZnS, and PbS have been synthesized into small quantum dot materials that have tunable emission in the visible and infrared (ir) wavelengths. The HgCdTe alloy system has been extensively studied for infrared photovoltaic detectors (4,5). Since, CdTe has a band gap of 1.49 eV and HgTe is a semimetal, the band gap of the alloy may be varied smoothly from over 1 eV to zero. Another interesting class of materials are the dilute magnetic semiconductors (6). The transition-metal Mn, with a half-filled d shell ($3d^5$), may be readily alloyed with all of the simple II–VI semiconductors. These materials have applications in flat-panel displays and are projected to apply to mid-infrared detectors and nonreciprocal optical devices (isolators and circulators). The Group 14–16 (IV–VI) lead salt crystals have a unique niche in mid-ir detectors and lasers.

This article focuses primarily on the properties of the most extensively studied III–V and II–VI compound semiconductors and is presented in five sections: (*1*) a brief summary of the physical (mechanical and electrical) properties of several compound semiconductors; (*2*) a description of the metal organic chemical vapor deposition (MOCVD) process. The MOCVD process is the preferred technology for the commercial growth of most heteroepitaxial semiconductor material; (*3*) the physics and (*4*) applications of electronic and photonic devices; and (*5*) the fabrication process technology in use to create both electronic and photonic devices and circuits.

2. Physical Properties

The defining characteristic of a semiconductor is that there is a gap between the completely filled valence states and the lowest excited or conduction states of the crystal. For many compound semiconductors, this range in energy between the valence and conduction states is < 2.5 eV. With the advent of wide band gap

semiconductors, however, this range in energy has been extended to almost 6.2 eV, which is the band gap of AlN (1).

A schematic band structure for a zincblende direct gap semiconductor is shown in Figure 1. The three lowest bands are valence, v, bands and the upper three minima derive from the lowest conduction, *c*, band. What defines the properties of electronic and photonic devices made from compound semiconductors are the positions of the valence band maximum and the conduction band minima in reciprocal space. For example, GaP has its lowest conduction band minimum at X and its valence band maximum at Γ_v, while for GaAs both the conduction band minimum and the valence band maximum occur at Γ. The alignment of the conduction band minimum and valence band maximum at Γ is what gives GaAs a direct bandgap transition and its wide range of applications. Because the minimum band gap is $\Gamma_c - \Gamma_v$, and noting that the momentum of a photon is negligible, light emission via the direct, momentum conserving recombination of electrons (in the conduction band) with holes (in the valence band) is possible. On the other hand, GaP has a similar band structure to Si and has an indirect bandgap transition. In indirect semiconductors, eg, Si and GaP, light emission is not readily obtained from recombination across the minimum band gap because momentum is not conserved in a simple photon emission process. For this reason virtually all LEDs and diode lasers are fabricated from compound semiconductors with direct band gap transitions.

The primary advantage of a direct gap semiconductor is its ability to strongly absorb and emit light at the fundamental band gap. The secondary advantage is that a small isotropic electron-effective mass is typically associated with the Γ_c minimum. The effective mass of an electron or hole in a crystal is inversely proportional to the curvature of the band in which it resides. In all zincblende semiconductors, the effective mass at Γ_c is nearly isotropic and universally less than the average of the anisotropic mass associated with either the L or X minima. It is also approximately proportional to the magnitude of the band gap. In GaAs the electron effective mass is $0.067\,m_0$, where m_0 is the free-electron mass. This may be compared to the electron conductivity effective mass of Si, which is $0.260\,m_0$. The effect of band structure on transport is illustrated by the electron velocity versus electric field curves for GaAs and Si shown in Figure 2. At low electric fields the steeper slope for GaAs implies an electron mobility roughly six times greater than in Si. This higher electron mobility results in shorter switching transients at lower voltages in field-effect transistors (FETs). At high electric fields, the electron transport in GaAs is limited by carrier scattering into the low mobility L minima resulting in a loss of this speed advantage. However, because the saturated velocity is obtained at much lower fields there is an advantage that GaAs FETs can operate at the same speed as a Si FET while consuming less power. This is a significant advantage for high density integrated circuits.

Another advantage of compound semiconductors is the ability to grow tertiary alloys (eg, AlGaAs) multilayer structures epitaxially, which can widely vary the material properties, such as band gap and refractive index from layer to layer. Within the constraint that the lattice constants are well matched it is usually possible to grow heterostructures of different III–V and II–VI semiconductors with atomically abrupt interfaces and monolayer thickness control. With

some intermixing at the interfaces it is also possible to grow lattice matched heterostructures between elemental, III–V, and II–VI semiconductors. For years, the Group III nitrides have been epitaxially grown on lattice mismatched substrates such as sapphire or SiC, resulting in material suitable for many device applications. Using a flexible growth system, the possible combinations of compound semiconductor materials are essentially infinite. This flexibility allows the design of a wide variety of complex devices by varying the electrical and optical properties and in many cases quantum size effects are exploited directly. The prevalent growth technologies are metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) (7,8). In MOCVD, deposition takes place on a heated substrate with the constituent elements are transported as metal-alkyls or hydrides in a hydrogen and/or nitrogen carrier gas. The carrier gas choice depends on its ability to be purified and its chemical inertness, however, growth in hydrogen may be beneficial to reducing impurities, eg, carbon and oxygen, in the semiconductor films. In MBE, deposition occurs in an ultrahigh vacuum by evaporating elemental beams from pyrolytic boron nitride crucibles that are resistively heated. Hybrid growth techniques can also be used, eg, the combination of metalorganics and hydrides in an MBE growth chamber. Other growth technologies which are less flexible than MOCVD and MBE are hydride vapor-phase epitaxy (HVPE) and liquid-phase epitaxy (LPE). These techniques can have faster growth rates but are limited in the specific materials that can be grown or in their ability to grow thin layers with abrupt junctions.

Table 1 lists the band gaps for many of the most common binary compound semiconductors. Also listed in Table 1 are the band gap transition type [direct (D) or indirect (I)], along with the crystal symmetry type [zinc blende (z) or wurtzite (w)], the lattice constant (one for zinc blende and two for wurtzite), the thermal expansion coefficient, and the bulk elastic modulus. Direct bandgap transitions occur when the valence band maxima and the conduction band minima both occur at the Γ symmetry point while indirect band gap transitions occur when the valence band maxima and conduction band minima occur at different symmetry points, eg, L or X. The thermal expansion coefficients and bulk elastic modulus are listed to show how the crystal structure expands as a function of temperature and elastically responds under applied pressure. The bulk modulus is only listed as an indication of the semiconductors compressibility and more advanced formulations are required to describe the details of how the materials respond elastically under applied stress. Understanding how the lattice parameters, thermal expansion coefficients, and elastic parameters influence the lattice is critical for the growth of defect-free heterostructures and either a uniform lattice constant must be enforced during growth or lattice mismatched layers must be constrained to be thin enough to allow purely elastic deformation, that are thermodynamically stable against plastic deformation. In the last two columns are listed the melting temperature and typical growth temperature. Note that in some cases the typical growth temperatures are only one-third or less of the melting temperature, which is especially true for the wider (larger) band gap materials.

In the design of heteroepitaxial layers, which are not lattice matched, the elastic constants of the layers are essential to the calculation of the thermo-

dynamically stable maximum layer thickness for elastic deformation, as well as the shape of the deformed unit cell. In most cases, the ⟨001⟩ surface is the preferred zinc blende crystal growth surface while for the ⟨0001⟩ surface is the preferred wurtzite crystal growth surface. For the zinc blende lattice, the deformation is purely tetragonal and expressions for the critical layer thickness and the dimensions of the unit cell are readily obtained (9). Due to the reduced symmetry of the wurtzite lattice the expressions for the critical layer thicknesses and crystal lattice distortions are more complicated. For growth on substrates with a different surface orientations high quality growth may be more difficult to obtain. An interesting case of lattice mismatched epitaxy is the case of a strained layer superlattice in which elastically deformed layers under compressive stress alternate with layers under tensile stress. By designing the magnitude of the tensile and compressive stresses to be equal, strained layer superlattices of arbitrary thickness may be grown with zero net stress, which is stable against plastic relaxation (10).

Along with the lattice constant the congruent sublimation temperature is a useful guide as to which pseudobinary alloys, $(AC)_x(BC)_{1-x}$ or $(AC)_y(AD)_{1-y}$, may be easily grown. Similar arguments apply to pseudoternary and pseudoquaternary alloys. When the lattice constants of the end-point binaries are closely matched the alloy is easily obtained for all mole fractions. Large lattice mismatches typically imply a miscibility gap in the alloy phase diagram. A large difference between the melting temperature and the typical growth temperatures also implies difficulty in growing high quality material. This is especially true for the Group III nitrides (GaN, AlN, and InN) where the growth temperatures are $< 1/3$ of the melting temperature (11). In the MBE process, the highest quality films are typically obtained at temperatures where the arrival rate of cation and anion fluxes is nearly stoichometric. For MOCVD, growth cation and anion fluxes are nearly stoichiometric for materials that contain more metallic cations and anions such as the antimonides and arsenides, however, for the materials where the anions are less metallic, eg, the phosphides, oxides, and nitrides, the anion fluxes can be significantly larger than the cation fluxes to make up for the anion desorption rates that occur during growth (11). Growth of alloy films is controlled to a large extent by the binary constituent with the lower growth temperature. A growth temperature near the lower temperature is required to ensure that all of the incident cation atoms are incorporated. On the other hand, a low growth temperature relative to the largest binary temperature enhances the formation of intrinsic point defects associated *with the high temperature component* of the pseudobinary alloy. Native defects usually have a deleterious effect on both the electrical and optical properties of the semiconductor.

Tables 2 and 3 list parameters that are useful in the design of electronic and photonic devices. The positions of the three lowest conduction band minima, E_Γ, E_L, and E_X, are given relative to the valence band maximum, which is universally at the center of the Brillouin zone, Γ. The conduction band minima with the lowest energy is in bold in this table. Also listed are the spin orbit coupling energy, Δ_0, electron effective mass at the Γ symmetry point, m_Γ, the Luttinger parameters, γ_1, γ_2, and γ_3, and the light and heavy hole effective masses, m_{lh} and m_{hh}. The valence band maximum is composed primarily of p symmetry

states derived from the anion. Spin–orbit interactions split what would be a threefold degenerate critical point into a twofold degenerate upper band and a nondegenerate lower band. Away from Γ the upper band splits into light and heavy hole bands. Neither of these bands has spherical constant energy surfaces and three Luttinger parameters, are required to describe the hole effective masses, m^*, in an arbitrary direction away from Γ. The relation is as follows where m_0 is the free-electron mass, k is momentum,

$$m_0/m^*_{ll(hh)}(k) = \gamma_1 \pm \left[4\gamma_2^2 + 12\left(\gamma_3^2 - \gamma_2^2\right)\left(k_x^2k_y^2 + k_y^2k_z^2 + k_x^2k_z^2\right)\right]^{1/2}$$

and k is a unit vector in momentum space. The plus sign refers to the light holes, lh, and the minus sign to the heavy holes (hh) (Table 2). For most calculations, the mass of the spin–orbit split-off band is unimportant and the light and heavy hole bands are approximated by directionally averaged parabolic bands. In many practical applications (12,13), this is accomplished by defining the parameter $\mu = (6\gamma_3 + 4\gamma_2)/5\gamma_1$. In this approximation,

$$mm_0/m^*_{ll(hh)} = \gamma_1(1 \pm \mu)$$

The relevance of the indirect minima E_{L} and E_{X} is in determining the transport properties of the material. For all of the Al compounds and GaP listed in Table 2, the lowest conduction band is at X and the valence band maximum is at Γ making $E_\Gamma > E_{\mathrm{L}} > E_{\mathrm{X}}$. This is the same relative ordering found in Si. The X minima may be approximately described by constant energy surfaces that are ellipsoids of revolution about the line of symmetry (denoted Δ) connecting Γ to X. Along Δ the longitudinal effective mass, m_l, is fairly large, on the order of $0.9–1.2\,m_0$. The transverse effective mass, m_t, in the plane perpendicular to Δ is usually $\sim 0.25\,m_0$. The conductivity effective mass is obtained as $m_c^* = 3/(m_l + 2/m_t)$. This is substantially larger than the isotropic Γ point effective masses obtained in the direct gap III–V semiconductors listed in Table 2. Here, the energy gap ordering is $E_{\mathrm{X}} > E_{\mathrm{L}} > E_\Gamma$ and $m_\Gamma = m_c^*$, which range from $0.014\,m_0$ for InSb to $0.079\,m_0$ for InP. It is because of the smaller effective mass in direct gap semiconductors that they are superior for the fabrication of high speed low power transistors. Similar properties are also true for the wurtzite direct bandgap semiconductors.

Table 3 lists several optical and electronic properties of the compound semiconductors listed in Table 1. These include the static dielectric constant, ϵ_0, and the index of refraction, n_∞. Typically, ϵ_0 and n_∞ decrease for increasing bandgap. The breakdown field, peak velocity, and electron and hole mobilities, μ_{e} and μ_{h}, are important for determining the speed of the electronic devices, but also their possible power output. For example, electronic devices made from GaN do not have as high a μ_{e} as devices made from GaAs, but they can be operated at much higher voltages resulting in 10 times the power output as described later. The last two columns of Table 3 list common dopants used to produce

n-type and p-type films. These are usually impurities that substitute on either the anion or cation lattice sites.

This high speed advantage of direct bandgap semiconductors over indirect semiconductors, including Si, diminishes as improvements in processing technology continue to shrink device dimensions. In long devices transport is dominated by the carrier mobility, which is inversely proportional to m_c^*. In short devices, performance is limited by the saturated drift velocity. Short devices imply large electric fields and electrons accelerated by the field are scattered into higher minima, primarily E_L, where they have a larger m_c^*. In this limit, the transport of electrons in direct and indirect semiconductors is very similar. In general, the performance advantage of a direct gap semiconductor in small device applications improves as the separations, $E_L - E_\Gamma$; and $E_X - E_\Gamma$;, increase. This criterion would seem to imply that semiconductors, eg, InAs and InSb, should make good transistors. There is a trade-off in that with decreasing E_Γ the electrons accelerated by the electric field quickly gain enough energy to interact with the lattice and break a bond releasing an electron–hole pair into the conduction channel of the device. This can lead to a runaway process known as avalanche multiplication which kills transistor performance. Most commercial transistors are made from GaAs, InP, and alloys with similarly large direct band gaps (Table 1).

Finally, due to the reduced lattice symmetry of the wurtzite semiconductors, spontaneous polarization exists in heterostructures, eg, AlGaN on GaN, due to the deviations from the ideal lattice constants at the heterointerface (14). At this interface, dipoles are generated resulting in a polarization field oriented along the *c*-axis [0001] direction. The magnitude of the polarization field is especially large for AlN–GaN interfaces due to the large difference between the spontaneous polarizations between AlN and GaN (14). Another polarization field in wurtzite semiconductors is the piezoelectric polarization, which is due strain generated at the heterointerface. Materials with larger lattice mismatch, eg, the Group III nitrides, will have larger magnitudes of piezoelectric polarization, since most heterostructures are likely strained. These two polarization fields result in net charge at the heterointerface, which can be advantageous for increasing the electron density in two-dimensional electron gas (2-DEG) structures and undesirable for electron and hole wave function overlap in quantum wells (QWs) in light emitting diodes (LEDs).

An extensive compilation of the properties of compound semiconductors may be found in the Landolt-Börnstein reference books (15,16) and also in Ref. 17. Various subvolumes in the series cover the properties of elemental, III–V, II–V, and other less common semiconductors. Information may also be found concerning semiconductor technology. Another useful source of information is the EMIS data review series (18). These books describe the properties and technology of GaAs, HgCdTe, InP, AlGaAs, InGaAs, and the III–V nitride compounds.

3. Metal Organic Chemical Vapor Deposition

Metal organic chemical vapor deposition (MOCVD) is a technique that has evolved since 1975 into one of the two prime growth methods for compound semiconductor devices. This is because of the capability to grow high quality, very thin layers of most III–V and II–VI semiconductors making it the most versatile of the growth methods in use. Many comprehensive reviews have been written on this technique (7,19,20). The MOCVD is also referred to as organometallic vapor-phase epitaxy (OMVPE), as well as MOVPE and OMCVD. Epitaxy is the term used to describe the growth by chemical reaction of a thin layer of semiconductor on the surface of a bulk crystal (wafer) of similar or different material, where the layer has a well-defined crystalline orientation with respect to the bulk crystal. The MOCVD growth typically involves decomposition in a cold wall reactor of chemical precursors, usually an organometallic Group III compound and a Group V hydride. For the growth of gallium arsenide [1303-00-0] from trimethylgallium and arsine, a typical reaction is as follows:

$$Ga(CH_3)_3 + AsH_3 \rightarrow GaAs + 3\,CH_4$$

While this chemical reaction explains the essential materials transformation, the details of the chemistry involved can be quite complex (21,22). This technique has been extended to all of the important III–V semiconductors, eg, AlGaAs, InP, InGaAs, and InGaAsP. In the past 10 years, the Group III nitrides have been successfully added to this list. Semiconductors grown by MOCVD for use as LEDs, lasers, solar cells, detectors, and high speed transistors are in commercial production. The MOCVD is a state-of-the-art technique for preparing epitaxial layers of compound semiconductors. It is a rapidly growing area as reflected by the number of papers and attendees at the biannual international conference. In 1981, 40 papers were presented at the international conference that had 112 attendees. In 1990, 199 papers were presented at the conference that was attended by 472 people. Topics of interest to researchers in MOCVD include the synthesis and use of novel sources, the continued improvement of the materials' purity, safe handling and monitoring of pryophoric and toxic precursors, understanding of the parameters that limit the sharpness of interfaces in heterostructures, the growth of quantum wires and dots, the reaction kinetics and growth mechanisms of MOCVD, ordered structures and how to control the ordering, the use of *in situ* diagnostics, eg, X-ray diffraction and optical reflection to control and better understand the MOCVD process, new reactor designs for multiwafer commercial growth, and extension of the technique to the growth of nonsemiconductors, eg, superconducting and ferroelectric oxide films (23).

3.1. CVD. Chemical vapor deposition is usually defined as a technique that involves a chemical reaction using molecular precursors that results in the deposition of a solid on a specific surface (24). Growth techniques, eg, MOCVD, chloride or hydride vapor-phase epitaxy, and gas source molecular beam epitaxy are considered to be CVD techniques. Growth methods, eg, liquid-phase epitaxy, molecular beam epitaxy, and sputtering, are not considered

CVD techniques because they lack one or more of the criteria in the definition. This technique offers the advantages of near equilibrium growth that allows for the precise control of growth rates and improved purity. The use of CVD allows one to utilize a growth pressure from atmospheric down to very low pressures ($<1.3 \times 10^{-3}$ Pa), as well as a large variety of reactants with widely varying chemical reactivities. Precursors that work especially well are gases or liquids with vapor pressures in the 0.1–100-Torr range. For liquid precursor delivery a carrier gas (H_2 or N_2) is bubbled through liquid to maintain a constant vapor pressure. Solid precursors that sublime can also be used, however, consistent delivery of the precursor may decrease over time if the solid sinters. To prevent the solid precursor from sintering, high molecular weight hydrocarbons can be added to the solid, to maintain constant molar delivery rates. *In situ* monitoring techniques, eg, uv fluorescence (25) or measuring the sound velocity of the metalorganic in the carrier gas (26) have been used to measure flow rates and improve the delivery consistency of the precursor.

MOCVD has demonstrated very precise and reproducible control of alloy composition, layer thickness, and dopant levels. The CVD techniques are generally readily scaled-up for mass production and reactors that hold 49-2 or 5-10 in. wafer are currently in use. Some disadvantages of the MOCVD technique include a large number of control variables, reactive atmospheres that can attack substrates and the growth apparatus, and the complexity of the apparatus, the mass transport, and the chemical reactions. Also, the reactor and all components must be constructed with materials that do not contribute impurities to the semiconductor films, and can withstand the MOCVD growth process. For this reason, many of the reactor components are made from stainless steel, quartz, SiC coated graphite, and other refractory materials.

A complete understanding of the MOCVD process at a fundamental level would necessitate knowing the thermodynamic and kinetic parameters for all of the possible species and reactions involved. As an indication of the size and complexity of the problem, a model has been presented for the growth of GaAs from TMGa and arsine that involves 24 chemical species and 45 reactions (27). For other compound semiconductors a complete reaction set may require more reactions. In spite of this complexity, a more limited set of thermodynamic and kinetic data may be used to predict trends that can be used to improve the control of the MOCVD process. Thermodynamic values are used to determine the equilibrium state for a given set of conditions and the driving force for a particular reaction. Thermodynamics can be used to determine the concentrations of reactants at equilibrium, to predict which reactants will yield improved results, establish trends for changes in process parameters, and predict maximum equilibrium growth rates. Kinetics describe the rate at which a reaction approaches equilibrium. Because MOCVD is not an equilibrium process, the actual growth rates and compositions of the resulting deposits are influenced by the kinetics, ie, reaction rates, mass transport, and the importance of individual reaction steps, of the system. Kinetics descriptions of growth may be more appropriate for growth conditions farther from equilibrium such as the wide bandgap semiconductors (11). For the MOCVD of GaAs, a complete thermodynamic and kinetic description is very complex (27). Most evidence indicates that surface adsorption of the reactants first takes place and then surface reactions occur to form the

semiconductor material under normal MOCVD growth conditions (20,27). For some growth conditions, the semiconductor may partly decompose during growth so that the surface desorption rate of the cations and anions must be compensated for during growth (11). In addition, adducts can form between the metal-organic and the hydride gas (eg, NH_3), leading to complicated gas-phase chemistry before any surface reactions even occur (28,29).

3.2. Transport Phenomena. One significant though often overlooked kinetic aspect of MOCVD is the influence that gas flow or hydrodynamics has on mass transport and uniformity of deposition. Because of the complexity of these effects, they are not intuitive and are often overlooked in the design of an MOCVD reactor. Both simplified and complete numerical descriptions of the hydrodynamics of certain types of MOCVD reactors have been published (7,19,30–32). These articles suggest reasons for using certain types of reactors, as well as design criteria that can be used to minimize the effects of temperature gradients, buoyancy driven circulation, and reactor boundaries. These effects are also more important the higher the growth temperature (Group III-nitrides and SiC) and if large flows of hydride gas (NH_3) are used during growth. The three types of reactors that are commonly used in MOCVD are pictured in Figure 3. The reactor types are commonly referred to as the vertical reactor, the planetary rotation reactor, and the horizontal reactor. The overall gas flow direction is indicated in each reactor. Another type of reactor geometry used in production is the barrel reactor, which can hold a large number of substrates. It is configured with a vertical flow, and the substrates are placed on the sides of a rotating substrate holder (19). Recently, simulations for GaN growth in a high speed rotating disk reactor model where the transition between buoyancy-driven flow and rotationally driven flow occurs (33,34), demonstrating that the potential for modeling the complex flow patterns can be understood and growth conditions that minimize turbulence and recirculation can be chosen. Effective modeling of reactor flow dynamics along with chemical modeling of the process is also essential for improvements in future reactor designs.

3.3. *In Situ* Diagnostics. Some of the complications that complex fluid flow causes in MOCVD can be overcome through the use of *in situ* diagnostic instrumentation. The use of *in situ* diagnostics is primarily aimed at reproducibility in growth rates and composition. These *in situ* techniques allow the grower to "view" the growth process and possibly make adjustments during growth to achieve consistent device layers. A number of techniques have been used as *in situ* monitors in MOCVD. These include X-ray diffraction using synchrotron radiation (35), ir, and uv spectroscopy (36,37), ellipsometry and reflection difference spectroscopy (38), spectral reflectance (39), ultrasonics (40), and mass spectroscopy (41). Some of these techniques are primarily for research and can be used to gain further insight into the reaction mechanisms of MOCVD; others, eg, uv spectroscopy, spectral reflectance, and ultrasonics, have been implemented into real-time process control. As the complexity of semiconductor structures increases the reliance on *in situ* process, monitoring will likely increase and will be highly desired by growers.

3.4. Materials. As understanding of the MOCVD process has increased, it has become possible through the synthesis of new chemicals to improve the uniformity and purity of materials grown by MOCVD and to increase the growth

parameter range over which device quality materials can be grown (42). Originally, the sources consisted of the trimethyl or triethyl Group III compounds and Group V hydrides. Because of the increased demand for improved materials and increased understanding, new chemicals have been designed that take into consideration the decomposition mechanisms of the sources and how this impacts on the incorporation of impurities, particularly carbon, into the epitaxial layer. The replacement of methyl Group III sources with ethyl groups has led to a marked decrease in carbon incorporation in AlGaAs grown by MOCVD (43), through the β-hydride elimination of the ethyl fragment from the surface (44). A further reduction of carbon can be achieved through the use of trimethylaminealane, which has no carbon bound directly to Al (45). Tertiary butyl arsine and phosphine are replacements for Group V hydrides that are highly toxic (46). Their use has resulted in the growth of high quality materials. In this case, the addition of carbon to the Group V atom has not resulted in increased carbon incorporation. This is explained by the decomposition mechanism that results in the formation of AsH_2. The AsH_2 reacts just like arsine on the growth surface and does not result in higher carbon incorporation (47). The use of new organometallic sources has increased researchers' process design parameters and will enable them to expand the growth capabilities of MOCVD.

3.5. Reaction Mechanisms. An integral part of the increased understanding of the MOCVD process has come about from a number of investigations into the reaction mechanisms for MOCVD. In a series of experiments (7) done to clarify the gas-phase decomposition of the Group III organometallics, it was found that the organometallics probably decompose predominantly on the surface through an interaction with other surface species. The existence of methyl and Group III radicals in the vapor phase has been demonstrated by ir and uv spectroscopies (36,37). Temperature programmed desorption indicates the presence of mono- and dimethylgallium on the surface of GaAs at temperatures $< 400^{\circ}C$. Evidence for the existence of methylene groups on the surface explains why only a small amount of the absorbed methyl groups incorporate as carbon into the growing epitaxial layer (48). X-ray diffraction patterns of the surface of GaAs during growth indicate that the surface reconstruction present during MOCVD is not the same structure as that found in MBE at high vacuum (49). This evidence can be explained using a reaction mechanism for MOCVD that involves the separate absorption of trimethylgallium and arsine onto the GaAs surface and their decomposition through a series of surface reactions (7,19). At high temperatures, the gas-phase decomposition of the reactants is an important side reaction.

The above reaction mechanism can be used to explain the observed growth rate behavior of GaAs (7,19). The growth rates for GaAs (and many other compound semiconductors) have three different temperature regimes (7,19,20). The low growth rates encountered in the low ($<500^{\circ}C$) temperature regime are explained by a lower decomposition rate of trimethylgallium on the GaAs surface. At an intermediate ($500-800^{\circ}C$) temperature, the growth rate is independent of temperature and limited by the mass transport to the surface. At higher ($>800^{\circ}C$) temperatures, the growth rate decreases with increasing temperature and reflects an increased rate of desorption of the reactants from the surface before they can interact to form GaAs (7,19). The effect of surface orientation

and arsine pressure on the growth rate is explained by the surface decomposition mechanism. Different surface sites that exist on different crystallographic orientations result in different decomposition rates (50).

The existence of methyl and methylene radicals on the surface during MOCVD growth explains the incorporation of C as an impurity. Other impurities that are typically found in MOCVD materials include O, Si, Ge, and Zn. The primary source of these impurities is the starting reactants. The incorporation of these impurities is dependent on growth temperature and V/III ratio. The growth conditions may play a larger role in carbon elimination from the surface during high temperature GaN growth and the simpler trimethyl precursors may lead to material with the lowest carbon impurity (51). Attempts to improve the quality of the material include the use of alternative sources as previously discussed and chemical purification of the sources. Great strides have been made by the chemical manufacturers over the years since the first MOCVD growths and chemical purity has improved dramatically; to the point where many impurities measured in the parts per million (ppm) levels are now measured in the parts per billion (ppb) levels. In spite of these impurities, high quality GaAs and InP have been grown by MOCVD with net carrier concentrations and mobilities as high as 210,000 and 300,000 cm^2/Vs, respectively.

3.6. Dopants. Some typical dopants for making n- and p-type material are listed in Table 3. Carbon has also been found to be an effective dopant for the III/Vs grown by MOCVD because of its relatively high solubility in Al-containing materials and its low diffusivity (7). Other dopant sources used in MOCVD include methyl or ethyl compounds Se, Te, Be, Zn, and Cd, and hydrides S and Se. Tetraethyltin and silane or disilane are also used as Group IV dopant sources. One unusual dopant source is bis(cyclopentadienyl magnesium), which is a p-type dopant for GaN and other the III/Vs. The Group VI sources are n-type dopants for the III/Vs, whereas the Group 2 and 12 (II) elements are p-type dopants. Both Si and Sn are usually n-type; carbon is usually p-type. However, because these elements can occupy either lattice site under some conditions they are amphoteric and can be self-compensating. The carrier concentration of the resulting doped layer is proportional to the partial pressure of the dopant source molecule. The variation of carrier concentration with temperature, growth rate, and V/III ratio depends on the incorporation mechanism for the individual dopant. Hydrogen has also been shown to compensate some dopants (52), especially Mg when it is doped into GaN. Hydrogen can usually be removed by annealing at high temperature and this has been studied extensively for p-type activation in Mg doped GaN (53).

For the III/V compound semiconductors it is typically easier to dope them n-type than p-type. This is because the acceptor levels lie deeper in the band gap than donor levels. This is especially severe in the wide band gap semiconductors, eg, GaN and ZnO. The acceptor activation energy for Mg in GaN is between 150 and 200 meV, meaning that Mg concentrations near $5 \times 10^{19}\,cm^{-3}$ are needed to produce hole concentration of $\sim 5 \times 10^{17}\,cm^{-3}$. As a result of the high impurity levels required for p-type doping in the nitrides, the hole mobilities are low, near 10–20 cm^2/Vs, as shown in Table 3. These lower hole concentrations can lead to lower photon production rates in LEDs and severely limit minority carrier based devices such as solar cells and photodiodes.

3.7. Heterostructures and Superlattices. Although useful devices can be made from binary compound semiconductors, eg, GaAs, InP, or InSb, the explosive interest in techniques, eg, MOCVD and MBE, came about from their growth of ternary or quaternary alloy heterostructures and superlattices. For the successful growth of alloys and heterostructures the composition and interface smoothness must be accurately controlled. The composition of alloys can be predicted from thermodynamics and kinetics. As previously mentioned, the surface reactions can be complex and lead to deviations from the predicted compositions. The temperature profiles and hydrodynamics of the reactor also affect the resulting composition from the effects of the transport of the reactants to the surface and the incomplete decomposition of the reactants. These effects are well illustrated by the GaAsP system where the amount of P incorporated varies dramatically with temperature due to the large difference in decomposition temperatures of arsine and phosphine (7,54). More severe effects are observed in the III-nitrides, where careful attention needs to be paid to gas-phase parasitic reactions that remove precursors from the growth surface (55). In addition, stress that increases as the heterolayer grows may limit the incorporation of the ternary compound (56). This effect is often referred to as compositional pulling and occurs in many situations.

Phase Separation. There are two common complications that occur when preparing ternary alloys of the III–V semiconductors. The first is the existence of a two-phase region in the phase diagram for the alloy of interest instead of a continuous solid solution. This results in phase separation or spinodal decomposition of the alloy. Phase separation occurs when the bond energy is very dissimilar between two of the constituents so that the entropy of mixing is not large enough to overcome the difference in the enthalpies of formation of the binaries and their solid solutions. This is expressed by a positive free energy of formation for the reaction of the two binaries to yield the desired ternary. Severe phase separation has been suggested to occur is the InGaN alloy, where compositions up to 6% of indium in GaN are thermodynamically stable and above 6% indium the InGaN phase separates into In- and Ga-rich regions [Ho and Stringfellow (56)].

Ordering in Ternary Alloys. The second complication is the existence of ordering in ternary alloys. Ordering, or the formation of a non-zincblende or non-wurtzite crystal structure, has been found to occur in most of the III–V alloys grown by MOCVD. The most common form of ordering in these materials results in a CuPt-like phase, where a superlattice with a translational symmetry of double the normal lattice occurs in the ⟨111⟩ direction. Ordering has a pronounced effect on the optical properties of alloys. Usually, the higher the degree of ordering, the lower the band gap. This can be advantageous in some instances where a lower band gap might be desired, eg, for long wavelength detectors in the InAsSb system, but deleterious in others, eg, AlGaInP, where shorter wavelengths are desired. Ordering is not observed for alloys grown by liquid-phase epitaxy (LPE) and probably results from the existence of reconstructions of the surface during growth that results in the preferential incorporation of different elements at different surface sites (7,57).

Abrupt Interfaces. The successful use of heterostructures in a device requires that they be prepared with abrupt interfaces. The growth of an abrupt

interface can be accomplished only by an abrupt change in the gas-phase composition. This can be accomplished by a growth interruption, the use of high flow rates, low growth rates, gas switching, and various combinations of these techniques. Through the use of gas switching sequences, one can prepare interfaces with a desired chemical composition. This is illustrated by the growth of InGaAsP on InP, where the interface can consist of InAs, GaAs, GaP, or various ternary bonds. These different interfaces result in different strain profiles at the interface and different electrical and optical properties for very thin layers (58,59).

The growth of thin superlattices and heterostructures with very abrupt layers and interfaces is probably the most significant development in MOCVD device technology. This ability has resulted in vastly improved device performance for lasers, high speed transistors, and detectors. This improvement resulted from the ability of MOCVD and MBE to grow heterostructures with low interfacial recombination velocities, which are directly related to the ability to prepare interfaces with very low defect densities that are nearly atomically abrupt (7). A transmission electron micrograph of a superlattice of alternating layers of InAsSb and InSb is shown in Figure 4. This high magnification micrograph indicates the sharpness of the interfaces that can be obtained with MOCVD. Monolayer abrupt interfaces have been claimed for GaAs–AlGaAs (7).

MOCVD is a very versatile growth technique with the capability of growing most of the III–V and II–VI semiconductors. High quality heterostructure devices using atomically abrupt layers have been prepared by MOCVD and are being produced commercially. The exploration of new material growth, growth mechanisms, uniformity, material purity, and large-area deposition will continue as the commercial applications of MOCVD expand.

Heteroepitaxy on Lattice Mismatched Substrates. As new semiconductor materials are developed there may not be a suitable substrate of that material to grow on. As a result, new materials are developed on chemically compatible substrates, which may be lattice mismatched making the crystal quality of semiconductor is less than ideal. No where is the lack of a suitable substrate more evident than in the growth of the Group III nitrides, which are typically grown on sapphire (16% lattice mismatch) or SiC (3.5% lattice mismatch). Despite the severe lattice mismatch and the resultant 10^8–10^9-cm^{-2} dislocation density, GaN of suitable quality can be grown such that bright LEDs can be produced, which surpasses the energy efficiency of incandescent lighting and equals that of fluorescent lighting. The GaN growth usually begins with a thin GaN or AlN nucleation layer grown near 550°C on the sapphire (60–62), which is heated to 1050°C under NH_3 to recrystallize the GaN to form nuclei (51) for further GaN growth at high temperature.

4. Electronic Devices

The main advantages that compound semiconductor electronic devices hold over their silicon counterparts lie in the properties of electron transport, excellent heterojunction formation capabilities, fast direct band-to-band electron-hole recombination, and semiinsulating substrates, which can help minimize

parasitic capacitances that can negatively impact device performance. The ability to integrate materials with different band gaps and electronic properties by epitaxy has made it possible to develop many different advanced devices. The hole transport in compound semiconductors is poorer and more similar to silicon. For this reason, the majority of products and research has been in n-type or electron-based devices.

Some of the original applications of compound semiconductors were in the development of diodes for microwave power and oscillator applications, including impact ionization avalanche transit times (IMPATTs) and transferred electron devices (TEDs). More recently, development efforts have focused on three terminal devices including heterojunction bipolar transistors (HBTs) and field-effect transistors (FETs). Presently, HBTs and FETs are the devices of choice for analogue, microwave, and digital circuit design in compound semiconductors. Much more recently, a newer class of devices called quantum effect devices (QEDs) has been the subject of intense research. The QEDs include resonant tunneling diodes (RTDs) and single-electron transistors (SETs). There is a great deal of speculation surrounding the functionality of these devices as present device geometries shrink to the range, where quantum effects are expected to dominate device behavior.

4.1. Diodes: Impatts and TEDs. Both IMPATTs and TEDs have been popular devices for use in microwave and millimeter wave power applications. These devices have been increasingly replaced by HBTs or FETs. Both devices are generally homostructures, using a single compound semiconductor, typically GaAs or InP (63). However, the doping profiles often make use of epitaxy, requiring sharp profile with low background and excellent control of low doping levels ($\sim 10^{15}\,\mathrm{cm}^{-3}$). Descriptions of IMPATTs and TEDs are available (63–65).

The IMPATT diode relies on the use of a nonuniform doping profile to tailor the electric field of a device under bias. A high electric field region is used to cause a local avalanche multiplication by impact ionization. A large drift region is then used to control the propagation of the carrier pulse. Figure 5(**a**) shows the doping and electric field profiles of an IMPATT device or Read diode (66). A direct current (dc) bias is applied to generate an electric field just below the critical field for impact ionization. A smaller alternating current (ac) bias causes the impact ionization to occur on the positive swing; on the negative swing the current is collected. This results in a 180° phase lag between the peak current and the positive peak in the ac voltage.

Transferred electron devices rely on the negative differential velocity inherent in the compound semiconductors with a second energy minimum that has a lower saturated velocity. Semiconductors that exhibit this behavior include GaAs and InP. An example velocity field curve is shown in Figure 2. The TED is biased so that the electric field is above the point where the maximum velocity occurs, E_t, or within the negative differential velocity regime. Figure 5(**b**) shows the doping and electric field profiles for a Schottky barrier contacted TED (63). Random charge fluctuations in the device result in a local space charge density that can propagate across the transit region of the device. A complete description of this phenomenon is available (65). As with the IMPATT, a combination of dc bias and an ac signal is used to initiate and propagate the charge pulse.

Although IMPATTS and TEDs are effective in producing microwave power at frequencies between 10 and 300 GHz, they are presently being replaced by FETs and HBTs. The reasons for this are twofold. Both IMPATTs and TEDs are extremely noisy when compared to FETs and HBTs, which can be a problem for many applications. The second issue revolves around integration. Both FETs and HBTs are being integrated into complete microwave circuits on a chip or millimeter wave-integrated circuits (MMICs). The advantages of this fabrication technology make FETs and HBTs the more attractive alternatives when possible.

4.2. Field-Effect Transistors. The basic operating principle of a FET is the modulation of a gate electrode bias controlling the current between two other electrodes, the source and drain, with minimal gate current. In silicon microelectronics, the metal oxide semiconductor FET (MOSFET) dominates the electronic device community. The gate or controlling electrode is separated from the silicon conducting channel by a thin oxide layer. This prevents any gate leakage current for all but the most severe operating conditions. In compound semiconductors, it has proven very difficult to fabricate a MOSFET-like transistor or a metal insulator semiconductor FET (MISFET). In a MOSFET, the insulator is silicon dioxide, which can form a well-behaved interface with silicon. The fabrication of a well-behaved or trap-free interface between an insulator and a compound semiconductor is difficult and has hampered efforts to produce MISFETs. Subsequently, compound semiconductor FETs rely on direct metal to semiconductor gates, and are much more likely to experience gate leakage at nominal operating conditions.

There are many ways to fabricate FETs in semiconductors with each separate technique employing a new acronym. Device types are divided as to how the electrons are confined in a channel, whether a semiinsulating barrier exists between the channel and the gate, and how the device is fabricated, ie, either self-aligned (SA) or nonself-aligned (NSA). One simple electrical distinction is whether the FET is conducting at zero volts on the gate. If a conducting channel exists between the source and drain when the gate voltage is 0 V, the device is said to be depletion mode or d-mode, requiring a negative gate voltage to turn the device off. If the device is off with 0 V on the gate, then the device is called enhancement mode or e-mode, requiring a positive bias on the gate to turn the device on.

Fabrication of FETs. Figure 6 shows the two basic geometries for compound semiconductor FETs, recessed gate and self-aligned. There are some similarities between the two structures. In both cases, it is desirable to make the source and drain ohmic contacts as low resistance as possible. Additionally, the material between the contacts and the gate represents a parasitic resistance that needs to be minimized or the device performance suffers. To accomplish this, the semiconductor is highly doped to achieve a low resistance. In a self-aligned FET [Fig. 6(**b**)] this doping is accomplished by ion implantation after the gate metal is in place. Because a high temperature anneal is required to activate the implant, the gate metal is usually a refractory metal, eg, tungsten. After implant activation the ohmic contacts are deposited and annealed. In the recess gate geometry [Fig. 6(**a**)] the semiconductor is made conducting by implantation/anneal or epitaxy before the metal contacts are in place. The source and drain contacts are then deposited and annealed to provide a low resistance contact.

Before deposition of the gate, a light patterned wet etch is used to thin the conducting layer. The same photoresist that is used to mask the wet etch is then used to define the gate metal lift-off. In this way, the gate is aligned to the recess, but is not self-aligned to the whole structure. Although the gate is shown midway between the source and drain contacts, varying the gate placement can have beneficial effects on such properties as breakdown and drain–source output conductance (67).

The channel region of the device is located directly below the gate metal. Except for fringing effects, it is the charge in the channel region that is modulated by a voltage applied to the gate. The semiconductor material beneath the gate can be homogeneous as in a metal semiconductor FET (MESFET) or junction FET (JFET), or it can be a heterojunction structure grown by epitaxy. In a MESFET, the gate is placed directly on the channel material, with the doping defined either by implantation or epitaxy. In a JFET, a p–n diode is used as the gate, with the gate contact acting as a ohmic contact to the p-region, in the case of an n-channel device.

Epitaxial devices usually enable shallower or sharper dopant profiles than are possible with implantation. This can be extremely important in very short gate length devices. Epitaxy is also used to exploit the properties of heterojunctions in a FET structure. Figure 6(**c**) shows the epitaxial structure for a typical HFET (heterojunction FET). There are many different ways of arranging the layers within a HFET. The two main approaches have tried to exploit modulation doping or semiinsulating layers. In a modulation doped structure, a wide band gap material is doped while a narrow band gap material is left nominally undoped. The dopants are placed within a few tens of nanometers (nm) of the interface. The electrons transfer to the lower band gap material, where high electron density can be achieved with spatial separation from the parent donor atoms. This allows the material to have high electron mobility that can improve device performance (68). Typical heterojunctions used include AlGaAs–GaAs and InAlAS–InGaAs. These devices are often called high electron mobility transistors (HEMTs) or modulation doped FETs (MODFETs). The amount of electric charge transferred to the lower band gap material is especially large in AlGaN/GaN based HEMTs due to the strong piezoelectric effect present in these device layers (14). The narrow band gap layer can be semiinfinite [see Fig. 6(**c**)] or a quantum well, with more wide band gap material below. Both approaches have advantages and disadvantages (69). In a different approach, the heterojunction is used to reduce gate leakage. If wide band gap material is left undoped, it acts as an insulator in a MIS-like structure. However, because the wide band gap material does have a finite conductivity and band gap, often small improvements in gate leakage are all that can be expected. In these cases, the channel doping is located within the narrow band gap material. These devices are often called heterojunction insulated gate FETs (HIGFETs) or doped channel FETs (DCFETs).

FET Device Characteristics. The current between the source and drain of a FET is the product of the electron density in the channel (below the gate) and the velocity of the electrons. The gate modulates this current by controlling the electron density in the channel. The velocity of the carriers can be controlled by increasing the bias on the drain, with the source typically grounded. When a

voltage is applied to the gate, the amount of charge on the gate is changed. In response to this, the charge in the channel redistributes. For n-type devices, a negative gate bias causes a depletion of the channel electrons, whereas a positive gate bias causes an accumulation of channel electrons. The situation is reversed for a p-type device with holes in the channel. A JFET works in the same way, with a p–n diode acting as the gate instead of a metal–semiconductor Schottky contact. The electrons in the device that are not under the gate are not modulated by the gate bias and populate connection paths between the channel and the source and drain ohmic contacts.

Although the relationship between the channel charge and gate bias can be complicated, it can be simply approximated as a capacitor structure. In this simplification, the following equation holds, where q is the electron charge, n_{ch}

$$Qn_{\mathrm{ch}} = C_{\mathrm{GC}}V_{\mathrm{GS}}$$

is the electron density in the channel, C_{GC} is the gate–channel capacitance, and V_{GS} is the gate–source voltage. Typically, this approximation is valid over the mid-range of operating conditions. At very low gate biases the device is said to be near threshold, the point where the device current turns on, and this relationship is no longer valid. At very high gate biases, the channel charge may saturate and the gate begins to leak. High performance devices try to modulate the most charge with the smallest changes in gate bias. This requires a high gate–channel capacitance, which is achieved by placing the gate close to the conducting channel.

The electron velocity within the channel is primarily controlled by the drain-to-source bias and the gate length. For very long devices (gate lengths $> 2\,\mu\mathrm{m}$), the electron velocity is equal to the product of the electric field and the mobility. In the long gate length regime the source-to-drain current can be expressed as follows, where $\beta = q\mu\epsilon W/2L_{\mathrm{G}}d_{\mathrm{GC}}$, L_{G} is the gate length, d_{GC} is

$$I_{\mathrm{DS}} = \beta(V_{\mathrm{GS}} - V_{\mathrm{T}})^2$$

the gate-to-channel distance, μ is the electron mobility, ϵ is the dielectric constant, W is the device width, and V_{T} is the device threshold that is dependent on the details of the doping (65). For short gate length devices ($< 1\,\mu\mathrm{m}$), the electric field due to the drain-to-source bias is very high and the electrons tend to travel at their saturated velocity, v_{sat}. When the electrons can be assumed to be traveling at their saturated velocity, the current is approximately the product of v_{sat} and qn_{ch}. Typical dc I–V characteristics are shown in Figure 6(**d**).

A popular metric of the speed performance of a FET is f_t, the maximum frequency of unity current gain (69). For short gate length devices operating at the saturated velocity this metric can be expressed as follows, where

$$f_t \approx gm/2\,\pi C_{\mathrm{G}} \approx v_{\mathrm{sat}}/L_{\mathrm{G}}$$

is the device transconductance, and C_{G} is the total gate capacitance. This implies that for high speed performance, short gate lengths and high saturated velocities are desirable. Extremely short gate length ($L_{\mathrm{G}} < 0.1\,\mu\mathrm{m}$) devices have exhibited f_t

values in excess of 300 GHz (70). More typical performance for 0.5-μm gate length devices is ∼30–60 GHz (69). This is the driving reason behind the constant decrease in FET gate lengths. Additionally, for digital applications the power consumption drops for shorter gate lengths. However, as the devices become shorter the scaling properties become very important. In order to maintain good modulation control of the channel, the channel doping needs to become shallower as the gate length is reduced. The ratio of L_G to d_{GC} needs to be maintained above four for good scaling behavior (69). Additionally, very short gate length devices have low breakdown voltages due to the very high electric fields present. This generally necessitates a trade-off between speed and power performance.

Because f_t is also proportional to the saturated velocity, significant effort has been made in developing materials with increased electron saturated velocity. This has included InGaAs on InP substrates and even InAs devices. However, the higher saturated velocity generally comes with a lower band gap that also implies easier breakdown. In addition to the concept of saturated velocity, there has been work in the area of ballistic transport. The device gate lengths are so short that the electrons do not have time to reach steady-state transport, and it is predicted that the electron velocity can greatly exceed the saturation values for short distances (65).

With both a higher breakdown field and peak electron velocity (as shown in Table 3), GaN-based HEMTs can produce power densities 10–20 times those of GaAs-based devices. The allows for the reduction in size of GaN-based components that increases the bandwidth over which the devices can operate while maintaining good matching to both input and output signals. Because of the higher breakdown fields GaN based-HEMTs can be operated at much higher voltates (<120 V) compared to GaAs (5–8 V), which allows for higher power handling and dramatic increases in power density (71). With a novel field plate design, GaN-based HEMTs have been fabricated with 32.2-W/mm output power. In addition, GaN-based HEMTs grown on SiC have the added benefit of 10 times the thermal conductivity of similar devices on GaAs, which reduces the need for active cooling of the devices during operation.

4.3. Heterojunction Bipolar Transistors. The FET and the heterojunction bipolar transistor (HBT) are the dominant electronic device technologies in compound semiconductors. Whereas the FET is operated as a voltage controlled current amplifier, the HBT is used as a current controlled current amplifier. Although the operating principles are quite different the output characteristics are similar in that a small control signal is used to switch a larger magnitude output signal on and off. The gain of the device is an attractive feature for both analogue and digital applications. There has been a great deal of discussion around the issue of whether HBTs or FETs are more suited to particular applications. However, it is sufficient to say that both devices are extremely useful and have application in a wide range of circuits.

In silicon technology, the HBT can be fabricated from Si–SiGe heterojunctions, but the homojunction Si bipolar junction transistor (BJT) is more common. The BJT and the HBT are nearly identical devices, with the HBT incorporating at least one heterojunction interface between device regions. Homojunction BJTs in compound semiconductors are not an area of active interest, as the

HBT offers large performance gains necessary for high speed and high power applications.

In an HBT, the charge carriers from an emitter layer are transported across a thin base layer and collected by a third layer called the collector. A small base current is present that includes the carriers that did not successfully cross the base layer from the emitter to the collector. The FET is a unipolar device making use of a single charge carrier in each device, either electrons or holes. The HBT is a bipolar device, using both electrons and holes in each device. The emitter and collector layers are doped the same polarity (n- or p-type), with the base being the opposite polarity (p- or n-type). An HBT with a n-type emitter is referred to as a n–p–n device; a p–n–p device has a p-type emitter. The n–p–n transistors are typically faster and have been the focus of more research. For the sake of simplicity, the following discussion will focus on n–p–n transistors.

HBT Design. The HBTs are similar to FETs in that poor fabrication can result in large parasitic resistance and capacitances that can dominate the device performance. As such, there are many different fabrication technologies for HBTs, making a complete overview impossible herein. Therefore, this discussion will focus on the more common aspects of HBT fabrication. A typical emitter-up HBT is shown in Figure 7(**a**). The layers are deposited by epitaxial techniques. In this example, the collector is deposited first, followed by the base, and then the emitter. There has also been work in collector-up structures in an attempt to minimize excess base–collector capacitance (72). In this example, the collector and base are of the same narrow band gap material, with a wide band gap emitter. Typical material combinations are AlGaAs–GaAs, InP–InGaAs, and InAlAs–InGaAs. This structure is referred to as a SH–HBT or a single heterojunction HBT. Devices have been fabricated that use a wide band gap material for the collector and are referred to as DH–HBTs or dual heterojunction HBTs. The use of a wide band gap material in the collector can increase the device breakdown voltage and therefore increase the maximum available power from the device.

The doping in both the emitter and collector are typically nonuniform. Near the region where an ohmic contact is made, the doping is raised to reduce any parasitic resistances. However, closer to the emitter–base or collector–base junction the doping is modified to provide the proper I–V characteristics of the individual n–p diodes. The base is typically thin (< 100 nm) and is very heavily doped ($>10^{19}\,\mathrm{cm}^{-3}$). This is to facilitate ohmic contact formation and lower the sheet resistance of the base layer. Most of the device action occurs directly under the emitter contact, and the base layer between the emitter contact and base contact acts as a parasitic resistance. The emitter layer is defined using either wet or dry etching, often with selective etches to ensure stopping in the correct place. The exact details are particular to the device technology, self-aligned versus nonself-aligned. Very high doping or self-aligned contacts are used to minimize this resistance. The very high doping of the base layer can often introduce unwanted dopant diffusion (73). This must be accounted for in the fabrication process, often by leaving a thin (< 10 nm) undoped layer between the base and emitter to allow for dopant diffusion (74). Because the emitter contact is typically very small, its contact resistance is of paramount performance. In addition to the metallization schemes discussed elsewhere, it is not

unusual to see the emitter layer graded down to a very narrow band gap material to facilitate ohmic contact formation (75).

The active region of an HBT is directly beneath the emitter contact, where the injected electrons cross the base and enter the collector. Because the emitter is etched away in regions to allow base contacting, the emitter–base junction is typically of minimum size. However, the same is not true for the base–collector junction. In addition to the region directly below the emitter, the entire length of the base out to the base ohmic contact forms a capacitor with the collector. This parasitic capacitance has a large negative effect on device performance. A technique for minimizing this capacitance is the use of ion implantation to isolate the collector region (76). By proper choice of ion and energy, it is possible to render the collector region near the base insulating, without significantly affecting the base resistance. This dramatically reduces the parasitic base–collector capacitance.

HBT Device Characteristics. The HBT consists of two back-to-back n–p diodes. In the most typical configuration, the emitter–base diode is forward biased, with the collector–base diode reverse biased. Because the current in a forward-biased n–p diode is exponentially dependent on the bias, small changes in the emitter-base voltage result in large changes in the emitter current. The current across the emitter–base junction is a combination of the electrons injected into the base and the holes injected into the emitter. If the diode was semiinfinite to each side, the electron current density, J_n, could be expressed as follows (64), where q is the electron charge, V is the bias across the diode, kT

$$J_n = \frac{qD_n n_{po}}{L_n}\left(\exp\left(\frac{qV}{kT}\right) - 1\right)$$

is the thermal energy, D_n is the electron diffusion coefficient in the base, L_n is the electron debye length in the base, and n_{po} is the equilibrium electron concentration in the p-type base material. The key aspects of this equation are (*1*) the current is exponential with bias and (*2*) the current is proportional to n_{po}. As the best performance results if all of the emitter–base voltage is dropped across the junction and the base layer is typically very thin, a heavy doped base layer is desirable to minimize the base resistance away from the junction. However, a large p-type doping in the base lowers n_{po} because $np = n_i^2$ (64), where p is the hole density and n_i is the intrinsic carrier concentration, which is temperature dependent. A high p-type doping density in the base, therefore, would result in a lower electron current and a higher hole current, exactly the reverse situation desired. However, if a heterojunction n–p diode is used, an additional barrier to the hole current comes from the valence band discontinuity (77). In this case, the ratio of the electron-to-hole current is as follows (77), where

$$\frac{I_n}{I_p} \approx \frac{N_E}{P_B}\exp\left(\frac{\Delta E_v}{kT}\right)$$

The parameter N_{E} is the emitter n-type doping, P_{B} is the base p-type doping, and ΔE_{v} is the valence band discontinuity. Valence band discontinuities are

usually in the range of 0.1–0.3 eV. Because the exponential can be very large, this allows the ratio of the emitter-to-base doping to vary considerably. This is helpful in allowing the base doping to be increased thereby lowering the base resistance. In addition to the hole current injected into the emitter, some of the emitter electron current suffers from recombination within the base layer that adds to the base current. Typically, this is a small fraction of the total current. A key parameter for HBTs is the current gain or β, which is the ratio of the emitter current to the base current. This can be a very large number in HBTs as it is proportional to the exponential of the valence band discontinuity. Typically, however, β is not maximized, as the overall structure takes advantage of the exponential to vary doping levels to reduce parasitic effects. Figure 7(**b**) shows an example of the dc characteristics for a common emitter HBT.

An approximation for the maximum frequency of unity current gain, f_t, in an HBT can be expressed as follows (74), where τ_E is the emitter charging

$$1/2\pi f_t = \tau_E + \tau_{BT} + \tau_{CT} + \tau_C$$

time, τ_{BT} is the base transit time, τ_{CT} is the collector transit time, and τ_C is the collector charging time. The emitter charging time, τ_E, can be expressed as the RC product of the emitter resistance and the emitter–base capacitance. The base transit time, τ_{BT}, is equal to the width of the base divided by the carrier velocity. The collector transit time, τ_{CT}, is equal to the width of the collector depletion region divided by the carrier velocity. The collector charging time, τ_C, can be expressed as the RC product of the base–collector capacitance and the collector series resistance. Although these equations are simplified, they do provide insight as to why the series resistances and excess capacitances are important to minimize. State-of-the-art HBTs have exhibited $f_t s > 100$ GHz.

4.4. Quantum-Effect Devices. As modern devices become smaller in pursuit of higher speed and lower power operation, they are entering length scales where quantum effects are expected to become important, if not dominant. Instead of trying to avoid these quantum effects in conventional devices, an alternative approach is to exploit these effects in developing new devices (78–80). Although conventional devices often improve with shrinking size, small dimensions are a requirement for the successful operation of quantum-effect devices (QEDs). This field is in its infancy with many issues to be resolved including how best to incorporate quantum effects into devices that can be used in a complete system. Because the behavior of a QED may be significantly different from conventional devices, work is also being carried out in system architecture issues, as the best way to utilize these unconventional devices is unclear (81). Many QED concepts have increased functionality over the basic on–off behavior of FETs or HBTs. This could allow the design of complicated systems with decreased numbers of devices thereby increasing speed and further reducing power consumption.

Electron tunneling is the basis for the resonant tunneling diode (RTD), a two-terminal device exhibiting on–off–on behavior. The RTD uses epitaxy to achieve the small dimensions necessary to control the tunneling, whereas the lateral dimensions can be $>1\,\mu$m, allowing conventional lithography to be used for fabrication. Other QEDs that use a horizontal geometry, relying on ultra

small lithography, include single-electron transistors (SETs) and electron interference devices. Single-electron transistors are devices in which the addition or subtraction of a single electron is sufficient to control the operation. There have been a number of other device technologies proposed in compound semiconductors that have yet to be proven experimentally. These include electron interference devices (82) and a novel technology for quantum cellular automata (QCA) (83).

4.5. Resonant Tunneling Diodes. The structure of a AlGaAs–GaAs resonant tunneling diode (RTD) is shown in Figure 8(**a**). Typical heterojunctions for RTD fabrication include AlGaAs–GaAs, InAlAs–InGaAs, and InAs–AlSb. The key component of the RTD is the thin double-barrier structure grown by epitaxial techniques. Typical length scales are ≤ 5 nm. Figure 8(**b**) shows the conduction band along the vertical direction through the double-barrier structure. The two AlGaAs wide band gap barriers form a resonance state in the confined GaAs layer. Electron transmission through the double-barrier structure is limited to those electrons that can conserve both energy and momentum as they tunnel from the emitter, through the barrier, and into the collector (84). Typical I–V characteristics are shown in Figure 8(**c**). Initially the electrons in the emitter do not have enough energy to tunnel to the collector and the current is low. At a bias of V_{pk} a large number of emitter electrons satisfy the tunneling constraints and can tunnel through the barrier, resulting in a high current. As the bias is further raised, the emitter and barrier fall out of resonance and the tunneling current reaches a minimum. With further bias increases thermionic emission over the barrier dominates. The key characteristics of the RTD are the peak current, I_{pk}, the voltage at peak current, V_{pk}, the minimum or valley current, I_V, and the voltage at the valley current, V_V. Investigations into InAlAs–InGaAs and Sb-based RTDs are based on the improvements on peak current and the peak-to-valley ratio (PVR) (85). The best room temperature PVRs of 11 have been achieved for InAs–AlSb (85). In general the improvements come from higher conduction band discontinuities between the barrier material and the confined well material. Lower temperatures also improve the sharpness of the tunneling characteristics due to the reduced thermal spreading of the electron distribution in the emitter.

The RTDs have exhibited microwave oscillations at frequencies in excess of 700 GHz (86). Unfortunately, the available power output is very low. Although circuit design with two terminal devices is more difficult than with three terminal devices, RTDs are being explored for use in digital logic (87), multivalued logic (88), memory circuits (89), and analogue circuits (90). Work is also in progress to develop three-terminal resonant tunneling transistors (RTTs) (69,82).

4.6. Single-Electron Transistors. The greatest potential application for single-electron devices lies in digital circuits. However, a number of other applications exist, including current standards and ultrasensitive electrometers (91,92). The SETs are not unique to compound semiconductors, and in fact a great deal of work has been carried out in other material systems, including Al–AlO_x–Al tunnel junctions. A review of single-electron phenomena is available (93).

The basic operating principle of a SET lies in how much energy is required to add or remove a single electron from the system. Figure 9(**a**) gives the

structure for an AlGaAs–GaAs SET. These devices are also referred to as Coulomb blockade devices. The AlGaAs–GaAs heterojunction is used to fabricate a vertically confined two-dimensional electron gas. Gates A, B, C, and D are then biased negatively to isolate region E from the surrounding electrons. Region E is typically very small ($<100\,\mathrm{nm}^2$) and is occupied by a small number of electrons ($\sim 1 - 1000$ s). The depletion regions formed between gates A–C and B–C act as the inlet and outlet for electrons traveling through region E. By lowering the negative potential on gates A or B, single electrons can be allowed to enter or leave region E. Modulating gate D allows the energy of the system (region E), to be modified. The energy to add or remove a single electron is $e^2/2C$, where e is the electronic charge and C is the total capacitance of the charge island (region E). If the island's electron occupancy is an integer, n, then there is a block to charge moving from region F to G. However, if the occupancy is $n + 0.5$, oscillating between n and $(n + 1)$, then it is possible for electrons to travel from region F to G. Additionally, because the electron occupation of region E is changed by the voltage on gate D, the conductance is periodic in gate voltage as shown in Figure 9(**b**).

Due to thermal effects such devices must operate at temperatures well below the electron charging energy of $e^2/2C$. With state-of-the-art fabrication technology, the capacitance is typically of the order 10^{-16} F, which requires temperatures < 1 K. Even with further miniaturization, it is unlikely that these devices will be feasible at room temperature. Even so, there has been work in modeling this type of device for use in digital circuits (94).

There is another class of SETs that do not make use of the energy to add single electrons to a system. These devices use the trapping of individual electrons to modify the conductance of a more conventional FET channel (95). By trapping charge in polysilicon grain boundaries, these devices have been operated at room temperature with very promising electrical characteristics. This device operates on the electron's ability to electrostatically deplete the channel, not on the energy required to trap the electron.

5. Photonic Devices

A technology for which compound semiconductors are uniquely suited is that of photonics, which describes devices that generate, amplify, detect, propagate, transmit, or modulate light. This field therefore covers a wide range of systems, including LEDs; lasers and optical amplifiers; detectors; waveguides, eg, optical fibers, lenses, and other optical components; and optical modulators. Although silicon has contributed much to photonics technology with its applicability to visible and near-ir light detection systems, the compound semiconductors, with their wide range of primarily direct bandages, enable the realization of efficient light-emitting devices, namely, laser diodes and LEDs, and extension of detector technology into the far-ir region of the spectrum.

The relevance of photonics technology is best measured by its omnipresence. Semiconductor lasers, eg, are found in compact disk players, CD–ROM drives, and bar code scanners, as well as in data communication systems, eg, telephone systems. Compound semiconductor-based LEDs utilized in multicolor

displays, automobile indicators, and most recently in traffic lights represent an even bigger market, with ~$1 billion in annual sales. Theoretically, LEDs are more energy efficient at producing light and they should ultimately replace traditional incandescent and fluorescent light bulbs. In fact a revolution in solid state lighting using compound semiconductors is currently underway with aggressive goals for increasing power efficiency and reducing cost. The trend to faster and smaller systems with lower power requirements and lower loss has led toward the development of optical communication and computing systems and thus rapid technological advancement in photonics systems is expected for the future. In this section, compound semiconductor photonics technology is reviewed with a focus on three primary photonic devices: LEDs, laser diodes, and detectors. Overviews of other important compound semiconductor-based photonic devices can be found in Refs. 96–99.

5.1. LEDs. A LED is a forward-biased p–n junction in which the applied bias enables the recombination of electrons and holes at the junction, resulting in the emission of photons. This type of light emission resulting from the injection of charged carriers is referred to as electroluminescence. A direct band gap semiconductor is optimal for efficient light emission and thus the majority of the compound semiconductors are potential candidates for efficient LEDs.

The most simple LEDs are homojunction devices, composed of the same bulk material with n- and p-type doped regions, as shown schematically in Figure 10(**a**). Greatly increased performance has been achieved with the development of heterojunction devices that combine two or more semiconductor materials of different band gaps. As shown in Figure 10(**b**), the different band gaps of the heterostructure enable the formation of potential wells in the junction region to better confine the electrons and holes that results in more efficient photon generation. Advances in semiconductor growth technologies such as MOCVD and MBE allow for the growth of more complex structures, eg, the multiquantum well structure, shown in Figure 10(**c**). In this structure, the center well of the double heterostructure LED is replaced with one or more very thin (< 10 nm) layers that result in further improved carrier confinement as well as changes in the energy and wavelength of emission.

In addition to the structural variations, there are also two principal LED geometries, namely, the surface- and edge-emitting geometries shown in Figure 10. For the surface-emitting LED, light is emitted in a direction perpendicular to the junction of the device. In most cases, this is the top surface of the device, although if the structure is grown on a substrate material that does not absorb the emitted photons, emission can be obtained from both the top and bottom surfaces of the device. In contrast, the edge-emitting LED emits light in a direction parallel to the device junction which, for a cubic crystal geometry, is usually cleaved $\langle 110 \rangle$ facets for a structure grown on a $\langle 100 \rangle$ substrate. This geometry is similar to that used for edge-emitting laser diodes and is generally less efficient than the surface-emitting geometry, and has an asymmetric beam profile. One clear advantage of the edge-emitting geometry is that it enables the development of superluminescent diodes that have greater output power and broader spectral output than surface-emitting LEDs.

Whether a particular LED will be useful in photonics applications depends critically on its wavelength, spectral bandwidth, external quantum efficiency,

and output power. The emission wavelength and spectral bandwidth are governed primarily by the band gap of the semiconductor materials that make up the LED, with larger band gap materials emitting at shorter wavelengths, because the band gap is inversely proportional to the wavelength, and generally narrower spectral line widths. The external quantum efficiency of the device is equal to the ratio of the produced photon flux to the injected electron flux and depends on both how efficient the material is at generating photons (internal quantum efficiency), as well as how efficiently the photons can travel from the junction and out of the material without being absorbed or reflected back (transmission efficiency). The total output power, P, of the LED is determined by the following relation,

$$P_0 = \eta_{ex} hcI/\lambda e$$

where I is the injected current in the device, c is the speed of light, e is the charge of the electron, h is Planck's constant, and η_{ex} is the previously described external quantum efficiency. Thus, for an ideal LED, the output power is proportional to the injected current.

The fact that compound semiconductors have a wide range of band gaps has enabled the development of LEDs from the uv to the mid-ir region of the spectrum. Starting at the shorter wavelengths, GaN is a Group III–V semiconductor material that is suitable for uv and blue-based LEDs (100). This new technology has overwhelmed the performance of commercial SiC-based blue LEDs with an order of magnitude improvement in output efficiencies (approaching 4%) and estimated device lifetimes as high as 100,000 h at an emission wavelength of 450 nm. Light-emitting diodes with wavelengths as short as 240 nm have been generated using suitable AlGaN alloys (55). Group II–VI materials based on ZnSe and more recently ZnO have also been proven to enable efficient LEDs in the blue and green regions of the spectrum, with significantly narrower spectral bandwidths than the GaN LEDs and slightly lower efficiencies (101,102). To date (~1996), the II–VI LEDs have suffered from shorter lifetimes than the GaN materials, with projected lifetimes of ~1000 h. One of the most important applications for these blue LEDs is that of multicolor displays. The GaN LED is in use as the critical third component of red–blue–green (RBG) multicolor displays, the other wavelengths having been developed previously out of other material systems.

LED technology in the rest of the visible region of the spectrum is dominated by GaP, GaAsP, AlGaAs, and AlGaInP materials. Although both GaP and GaAsP are indirect gap materials, they are often doped with impurities to enhance radiative efficiency, typical examples being nitrogen-doped GaP (GaP:N), zinc and oxygen-doped GaP (GaP:Zn,O), and nitrogen-doped GaAsP (GaAsP:N). These GaP and GaAsP LEDs span the deep red (700 nm for GaP: Zn,O) to the green (555 nm for GaP). Although not extremely efficient (external quantum efficiency for 630-nm red GaAsP:N, 0.1% for 555-nm green GaP), these materials compose up to 90% of the LED market because they can be grown with the mature and cost-effective technique of liquid-phase epitaxy (LPE) (103). AlGaAs-based LEDs are appropriate for long wavelength visible (650–700 nm) LEDs, and are used in traffic lights and car tail-lights. External quantum

efficiencies of >16% have been achieved at 650 nm. Direct gap AlGaInP materials, which cover the red to green regions of the spectrum, are promising for shorter wavelength visible LED applications (103,104). Significant advances in AlGaInP-based LEDs have been made by bonding the material to a transparent GaP substrate to enable light emission from both sides of the device (105). This technology has resulted in LED performance that exceeds all other commercial technologies for the green-to-red spectral regime. However, to ultimately use these LEDs for Solid State Lighting (SSL) applications great improvements need to be made in the internal and external quantum efficiencies, especially at the blue and yellow wavelengths where the eye is most sensitive.

The visible LEDs dominate the LED market, but longer wavelength LEDs also have applications. Near-ir LEDs (780–1000 nm) are used in short haul communication systems and are typically made of GaAs, AlGaAs, and InGaAs materials. The 1.1–1.6-μm region of the spectrum is also relevant for optical communication systems and LEDs emitting in this region are based on InGaAsP materials. Finally, InAsSb and related alloy structures have been developed into LEDs covering the mid-ir (2–5 μm) region of the spectrum. These wavelengths are useful for gas monitoring systems, such as those used to monitor pollution.

Beyond these commonly used double-heterostructure (DH) surface-emitting LEDs, there are several more advanced LED systems. Resonant cavity LEDs (RCLEDs) are structures where the light-emitting (active) region is grown in between two semiconductor-based mirror stacks, thus forming a resonant optical cavity (106,107). Typically, the cavity is highly asymmetric, with one mirror having a reflectivity close to 100% while the other has a reflectivity of typically < 97%. The effect of the cavity is to restrict the spectral bandwidth of the light emission to one of the modes of the cavity and also to enhance the light emission from the LED. Thus, RCLEDs can have higher spectral purity and higher intensities than standard LEDs and may be used in applications such as short-distance fiber optic communication systems, where narrower spectra translate to less dispersion in the optical fiber. Particular examples include visible (670 nm) AlGaInP-based RCLEDs (108) and InGaAs-based 940-nm RCLEDs (109), both designed for a spectral width of ∼5 nm.

Other applications, eg, wavelength division multiplexing (WDM) and some spectroscopic applications, require high powers and/or a broader spectral width than typical LEDs. In this case, a superluminescent LED is used, which typically has an edge-emitting geometry with cleaved facets and is essentially the same structure as a laser diode. The difference is that some loss mechanism, usually in the form of a tilted mirror or an absorbing region along the length of the LED, is introduced that prohibits the device from actually lasing. This allows a relatively high level of current injection without lasing, such that much higher powers and broader spectral outputs are achieved than from standard LEDs. Superluminescent LEDs have been reported throughout the near-ir region of the spectrum (110–112) and are sold commercially. At the communication wavelengths, as an example, 80- and 140-nm line widths have been achieved at 1.3 and 1.5 μm, respectively (111).

5.2. Lasers. First developed in 1962, the semiconductor laser diode has rapidly matured to become the dominant laser source used in photonics technologies, primarily due to its small size, low power requirements, manufacturability,

and robustness (113–115). Just as for LEDs, the wide array of primarily direct band gap compound semiconductors has enabled semiconductor laser development from the blue to the mid-ir region of the spectrum. The semiconductor laser diode is similar to the LED in that it utilizes the injection of charged carriers to emit light. In addition, the laser diode employs an optical cavity formed by mirrors, often just the cleaved facets of the semiconductor, to allow for optical feedback. The optical feedback enables stimulated emission to occur, in which reflected photons stimulate the emission of additional photons of the same energy and phase. Injecting current into the device provides gain to the system which is the mechanism that allows for the multiplication or amplification of photons. The photons that travel in the cavity also experience a certain loss, due to absorption in the cavity or transmission through the mirrors. When the gain of the laser system is greater than the loss of the system, lasing occurs.

Because lasers are governed by stimulated emission, their properties are distinct from those of LEDs, which emit spontaneous emission. In particular, the fact that stimulated emission generates photons of equal phase is responsible for lasers having coherence. This is important for applications, eg, holography, and enables improved focusability of light. As the mirrors of the cavity determine a preferred direction for photon propagation, the laser emission is in the form of a well-defined beam, as opposed to the isotropic emission from LEDs. In contrast to the relatively broad spectral output of the LED, the laser has one or more sharp emission lines, arising from optical modes that propagate due to the boundary conditions imposed by the laser cavity. Finally, the fact that the losses of the cavity must be overcome before lasing can occur results in a well-defined threshold injection current below which lasing cannot occur.

Several heterostructure geometries have been developed since the 1970s to optimize laser performance. Initial homojunction lasers were advanced by the use of heterostructures, specifically the double-heterostructure device where two materials are used. The ability of the materials growth technology to precisely control layer thickness and uniformity has resulted in the development of multiquantum well lasers in which the active layer of the laser consists of one or more thin layers to allow for improved electron and hole confinement as well as optical field confinement.

Like the LED, the laser diode has both edge- and surface-emitting geometries, with edge-emitting lasers being by far the most common. For the edge-emitting laser, light propagates in the plane of the wafer and the mirrors are typically fabricated by cleaving the wafer along a crystallographic plane. Although the reflectivity of these cleaved mirrors is only $\sim$30%, it is sufficient to support lasing in broad area lasers that have high gain. To reduce mirror loss, the facets can be coated with a dielectric multilayer stack to enhance reflectivity of the mirrors. The cavity length of edge-emitting lasers is usually on the order of 250–1000 μm.

Another type of edge-emitting laser commonly used in communications applications is the distributed feedback (DFB) laser. In this device, the cleaved mirrors that are commonly used are replaced by corrugations fabricated in the semiconductor material, as shown schematically in Figure 11. These corrugations result in a periodic refractive index variation that enables coherent feedback of the light propagating in the cavity (116). This complicated mirror has

definite advantages over a cleaved mirror in that it only allows one of the many optical modes of the laser cavity to propagate, resulting in single-mode (therefore single-frequency) output. As the optical fibers used in communication systems have significant wavelength dispersion at 1.55 μm, the sharp spectral profile of the DFB laser results in less distortion of the optical signal.

The surface-emitting laser geometry has two basic designs. One is an in-plane laser similar to that of an edge-emitting laser, but that uses some form of reflection to direct the light output perpendicular to the plane of the laser cavity. An example of this is shown in Figure 12(**a**) where etched 45° mirrors are fabricated at the output facet of an edge-emitting laser to direct the light. This type of laser is often referred to as a PCSEL. The other design, a surface-emitting design that is distinctly different from the edge emitter, is the VCSEL for which both the cavity and light propagation is perpendicular to the plane of the wafer [Fig. 12(**b**)] (117). The cavity is typically designed to be λ/n in thickness, where λ is the laser wavelength and n is the material index of refraction at that wavelength. This translates to ~200 nm (2×10^{-7} m) for a visible emitting VCSEL. Because the cavity is so thin, the photons do not experience much gain as they propagate through the cavity. Therefore, the losses in the system, particularly the mirrors, must be very small.

To achieve low loss, multilayer semiconductor mirrors are grown on each side of the laser cavity. Each layer is of thickness $\lambda/4n$ to form a coherent reflection of light at a designed wavelength, and as many as 50 layers are needed to achieve reflectivities on the order of 99.99%. These mirrors are called distributed Bragg reflectors (DBRs) and are one of the critical components of the VCSEL. Although VCSELs typically are not as high power as edge-emitting lasers, they have several advantages due to their vertical geometry. These include a circular, low divergence beam that is optimal for coupling to optical fibers, amenability to dense two-dimensional array fabrication due to their geometry, and the ease of wafer level testing because cleaving is not necessary to create mirrors.

Compound semiconductor-based laser diodes operate in the blue–green, red, and near- to mid-ir region of the spectrum. One of the areas of most recent developments is that of blue–green laser diodes. Interest in these short wavelength lasers arises primarily from optical data storage applications, where the shorter wavelengths translate to the ability to read or write more information on a disk. In early 1996, Nichia Chemical Industries reported the first demonstration of a room temperature GaN-based laser diode, with emission at 415.6 nm in the blue region of the spectrum (118). The GaN-based lasers will be used in the next DVD format and allow up to four times the storage capacity compared to the current DVD standard capacity. The GaN-based materials field is rapidly advancing and improvements in GaN laser diode performance, as well as expansion into the uv and green regions of the spectrum may be seen in the near future.

Another material system for which blue and green laser diodes have been demonstrated is that of ZnSe and related Groups II–VI materials (3,119). These II–VI materials are primarily grown by molecular beam epitaxy (MBE). The first demonstration of electrically injected blue–green edge-emitting lasers, observed at low temperatures and under pulsed conditions, occurred in 1991 (120). Rapid progress has extended the technology to room temperature continuous wave (CW) emission in the blue–green region of the spectrum (510–520 nm) (121–123),

with pulsed operation down to ~463 nm (124). One problem with these II–VI-based laser diodes is that they suffer irreversible degradation with CW lifetimes on the order of 1 h (125). The ZnSe-based VCSELs have been demonstrated with optical pumping (126,127).

As of early 1996, commercial laser diodes were restricted to emission in the red region of the spectrum. The dominant material for red laser diodes is AlGaInP, which has demonstrated room temperature pulsed lasing in broad area lasers down to emission wavelengths approaching 610 nm (128), with longer wavelengths (670–690 nm) giving significantly better performance. The AlGaInP high power laser diode arrays have been developed with up to 12 W emitted at 640 nm (129). Red VCSELs were first achieved from AlGaInP materials in 1993 (130), with more recent performance at 690 nm of up to 8-mW output power (131). Applications for red lasers include laser printers, bar-code scanners, optical data storage systems, and plastic fiber-based communications systems.

The materials GaAs, AlGaAs, and InGaAs are used in laser diodes with emission from 750 to 1000 nm. One of the principal technologies in this wavelength region is that of compact disk players and CD–ROM drives, which use 780-nm AlGaAs DH lasers (113). Although these lasers have become an industry standard, other materials have been developed to generate lasing in this wavelength region. One such material is the quaternary InGaAsP grown on GaAs substrates, which can be grown to cover the same band gap range (1.42–1.92 eV or 870–650 nm) as the AlGaAs materials (132). Near-ir semiconductors are also employed to pump erbium-doped fiber amplifiers that are used in long distance communication systems. The InGaAs lasers are used to supply the 980-nm laser emission wavelength, which is optimal for absorption into the doped fiber. Although the wavelengths of these 780–980-nm lasers are not optimized for fiber-based communication systems, they are routinely used as a low cost solution for short distance communication applications as well.

Near-ir (750–1000 nm) VCSELs based on GaAs, AlGaAs, and InGaAs materials are the most mature of the VCSEL technologies, and dramatic improvements in device performance have been achieved just through 1995. At present, InGaAs-based 980-nm VCSELs have been demonstrated with >50% electrical to optical power conversion efficiency (133) and threshold currents <100 μA (134,135). Output powers as high as 23 mW have been obtained (136). Advances in GaAs-based 850-nm VCSELs include CW output power of 59 mW from a 40-μm diameter device and lasing up to 200°C (137).

The most important laser wavelengths for communication applications is the 1.1–1.7-μm region in the near-ir. This arises from the fact that glass optical fibers used in data communication systems have minimum dispersion at 1.3 μm and minimum loss at 1.55 μm. The primary material system for laser diodes in this wavelength region is InGaAsP grown on InP substrates, where $In_{0.73}Ga_{0.27}As_{0.58}P_{0.42}$ and $In_{0.58}Ga_{0.42}As_{0.90}P_{0.10}$ alloys are used to achieve emission at 1.3 and 1.55 μm, respectively. The AlGaInAs alloys on InP substrates have also been used to achieve lasing in this region (138). The VCSELs have been demonstrated both at 1.3 (139) and 1.55 μm (140) since 1994, although the room temperature output powers remain low.

Laser sources that emit in the mid-ir region of the spectrum (2–5 μm) are useful for detection of trace gases because many molecules have strong

absorption bands in that region. Other applications include remote sensing and laser radar. Semiconductor lead–salt (IV–VI) lasers that operate CW at a temperature of 200 K and emission wavelength of 4 μm are commercially available; however, they have relatively low output powers (< 1 mW) (141). Group III–V quaternary materials have also been developed as mid-ir laser diodes, with the strained quantum well GaInAsSb–AlGaAsSb laser demonstrating up to 1.3-W CW output power at 2 μm (142). Many other ternary and quaternary III–V structures have been developed to enable longer wavelength emission. InAsSb–AlInAsSb strained quantum well structures are one example, with CW lasing at 3.9 μm achieved up to an operating temperature of 128 K (143).

5.3. Detectors. Whereas there are several types of photon detectors, the most common compound semiconductor-based devices are photoconductors and photovoltaic devices (96,97,144). With the photoconductive detector, a change in the resistivity of the semiconductor material as light is absorbed is measured. The spectral range of detection is limited on the long wavelength end by the semiconductor band gap (intrinsic detectors) or the binding energy of an impurity in the semiconductor (extrinsic detectors) and the current–voltage characteristics are nominally linear. The photovoltaic devices, often called junction devices or photodiodes, employ a p–n junction. The long wavelength limit of detection is determined by the band gap of the semiconductor material for most types of detectors. The intersubband detector is an exception. The absorption of light results in the generation of electrons and holes that are subsequently swept out of the depletion region of the junction. This carrier transport acts to forward bias the junction and to produce either an open-circuit voltage or a short-circuit current, which is measured. The current–voltage characteristic is not linear, but rather shows rectifying behavior (144). Many of the semiconductor materials that are used in detectors, eg, InSb, InAs, HgCdTe, PbTe, PbSe, and PbTe, have been developed as both photoconductive and photovoltaic detectors.

The most critical parameters that govern the performance of the detector are quantum efficiency, responsivity, and response time. The quantum efficiency, η, is the probability that a photon incident upon the detector will generate an electron–hole pair that contributes to a detectable current. Factors, eg, the reflection of the photons from the surface of the detector, generation, and recombination of the electron–hole pair outside of the junction, and absorption efficiency of the material reduce the quantum efficiency from the theoretical limit of 1. The responsivity R is a related parameter that relates the incident photon flux to the electric current and is measured in W/A. Finally, the response time of the detector is simply the time it takes for the current to be generated and depends on factors such as the resistance and capacitance of the photodiode and drive circuitry, and the mobility of carriers in the material. As detectors are often called on to operate in high speed applications, the response time of the detector is a critical parameter. Many applications, including high speed data communication systems, require the detector to respond to the intensity variation of light that is modulated up to a frequency of (10^{10} Hz).

Silicon-based detection systems are the dominant technology for single-element and array detectors in the near-uv to near-ir spectral region (350–1000 nm), with a quantum efficiency at least 20% greater than that of compound

semiconductors (approaching a value of 1 in the 700–800-nm range). The advantage of compound semiconductors is that they can cover a much wider spectral range than silicon, operating from the uv to the far-ir region of the spectrum. Applications for long wavelength ir (LWir) detectors that operate in the 8–12-μm region are numerous and include systems for navigation, weather, and pollution monitoring, remote sensing, night vision, and navigation. The most commonly used material system is HgCdTe–CdTe that operates in the 3–17-μm region of the ir and is utilized in commercial imaging arrays (145). Mid-ir detection is accomplished by InSb arrays, and near-ir detector technologies include InGaAs–InP materials that operate in the 1.3–1.6-μm region (145,146). Additional near-ir materials are quaternary materials, eg, InGaAsP–InP and AlGaAsSb–GaSb, which operate in the 0.9–1.7-μm region.

Developments have also been made on GaAs–AlGaAs quantum well ir photodetectors (QWIPs) (147). The GaAs has a large band gap with respect to InSb and HgCdTe, and does not absorb ir radiation longer than ~900 nm by direct band gap absorption. However, a GaAs multiquantum well structure can be designed that has confined energy levels only a few meV apart (115). This allows for the resonant absorption of ir radiation equal in energy to the energy separation between the excited energy state and the ground state of each of the quantum wells, as shown schematically in Figure 13. Because the energy spacing can be controlled by the thickness of the quantum wells, the detection wavelength region can be tuned to relatively long wavelengths. As an example, InGaAs–GaAs QWIPs have been developed with detectivity out to 19 μm (148). Although HgCdTe-based detectors still have higher detectivities at longer wavelengths ($\lambda > 8\,\mu m$) and at operating temperatures in the 4–77 K region, the GaAs-based QWIPs show higher detectivity at temperatures below 40 K (149).

Many of these material systems have been developed into avalanche photodiodes (APDs), which involve not only the generation of carriers with the absorption of light, but also the amplification of the generated carriers (96,97). This is accomplished by applying a very high reverse bias to the detector, resulting in a high enough internal electric field inside the material to generate additional carriers by impact ionization. These detectors therefore have a higher responsivity than more conventional photodiodes, but suffer from increased noise.

As for LEDs, substantial improvement in detector performance can be achieved by placing the LED structure inside a resonant cavity. In particular, the resonant cavity photodetector can achieve high quantum efficiencies in a relatively narrow spectral region (107). In one study, a mirror was designed to allow for resonant absorption of two wavelengths: 730 and 910 nm (150). This type of multiple wavelength detector shows promise for wavelength division multiplexing (WDM) systems where wavelength multiplexing enables enhanced transmission capacity.

6. Device Fabrication Technology

6.1. Wet Etching. Compound semiconductor processing makes extensive use of etching for, eg, active area definition, gate recess etching, and waveguide formation. Wet etching can provide a clean, damage-free surface with good

control of both etch depth and lateral undercut. Most wet etches are isotropic, which may limit their usefulness in high aspect ratio submicrometer applications where straight wall profiles are required. With the proper combination of semiconductors and etchants, excellent selectivity can be achieved to extend the utility of wet etches to the nanometer range. A guide to semiconductor etching can be found in Ref. 151.

Etch Profiles. The final profile of a wet etch can be strongly influenced by the crystalline orientation of the semiconductor sample. Many wet etches have different etch rates for various exposed crystal planes. In contrast, several etches are available for specific materials that show little dependence on the crystal plane, resulting in a nearly perfect isotropic profile. The different profiles that can be achieved in GaAs etching, as well as InP-based materials, have been discussed (152–154). Similar behavior can be expected for other crystalline semiconductors. It can be important to control the etch profile if a subsequent metallization step has to pass over the etched step. For reliable metal step coverage it is desirable to have a sloped etched step or at worst a vertical profile. If the profile is reentrant (concave) then it is possible to have a break in the metal film, causing an open defect.

A powerful feature of wet etching is the ability to achieve excellent etch selectivities of one material over another. This can be extremely useful in the fabrication of epitaxial devices with different material layers. Because selective etching allows the removal of specific layers, the final accuracy of the etch can approach that of the epitaxial layers. Etch selectivities of $>100{:}1$ have been achieved for citric acid: H_2O_2 etching of GaAs–AlGaAs and InGaAs–InP structures (155).

Etch Mechanisms. Most wet etches for the compound semiconductors employ oxidation of the semiconductor followed by dissolution of the oxide. For this reason, many wet etches contain the oxidant hydrogen peroxide, although nitric acid can also be used. One advantage of wet etching over dry is the absence of subsurface damage that is common with dry etching. Metal contacts placed on wet-etched surfaces exhibit more ideal characteristics than dry-etched surfaces.

Etch Chemistries for Compound Semiconductors. There is a great diversity in the number of wet etches used for compound semiconductors. By choosing the correct etch the result can be highly selective or completely nonselective, etching through multiple epitaxial layers with nearly constant rates. The profile can be isotropic or depend on the crystal orientation. Most photoresists do a fairly good job of withstanding the wet etches. However, if a dielectric or metal surface is to be exposed during the etch it is important to consider parasitic etching of these materials (156). The large number of etchants available for compound semiconductors is extensive and therefore only a limited number of them are listed in Table 4. Several references for the wet etching of GaAs and InP are available (157,158).

6.2. Dry Etching. For certain applications, dry etching has gained popularity over wet etching because of its increased control of etch profiles, attaining submicrometer features and the ability to introduce *in situ* monitoring capabilities into a dry-etch system. In general, dry etching of III–V semiconductors involves exposing the semiconductor to a directed energetic reactive plasma,

which etches the semiconductor through a combination of physical and chemical processes. Different etch systems and/or conditions can be used to vary the amount of physical or chemical etching. Ion-beam milling involves the purely physical sputtering action of argon atoms, while reactive ion etching (RIE) can have a very strong chemical component with highly isotropic profiles.

Dry-Etching Systems. The fundamental operational characteristic of a dry-etch system is the exposure of a semiconductor sample to energetic reactive gases. The gases that are introduced into the etch system have a large impact as to whether the etch has any chemical component or is a purely physical etch, as in ion milling. The pressures used are generally (0.1 mmHg) in order to reduce gas-phase interactions, increase the mean free path of the energetic gases, and control lateral etching. Very anisotropic etching usually occurs with pressures < 1.33 Pa and dc biases >100 V. A plasma is generated in the etchant gases by several techniques, including radio frequency (rf) energy, microwave energy, and microwave energy combined with magnetic confinement. The plasma may be located remote from the sample or the sample may be directly within the plasma.

Ion-beam milling is a dry-etch process that is 100% physical, using argon plasmas in a highly energetic mode of operation. Chemically assisted ion-beam etching (CAIBE), reactive ion-beam etching (RIBE), and electron cyclotron resonance (ECR) etching are similar in that the plasmas are located remotely from the semiconductor. Systems that remove the sample from the plasma in a downstream mode allow excellent independent control of the physical and chemical components of the etch. Inductively coupled plasma (ICP) etching and reactive ion etching have the sample sitting directly in the plasma. However, ICP etching allows decoupling of the ion density and ion energy, resulting in excellent control over the etch characteristics.

The physical component of the etch can cause damage to the semiconductor surface (169). Although this damage can often be annealed out at low temperatures, this is not always possible in the fabrication sequence. Additionally, in some cases it is necessary to use a wet etch to remove a thin damaged layer formed during a dry etch. If the etch is designed to have a chemical component then the atomic species in the plasma interacts with the semiconductor forming volatile by-products that desorb from the surface. The sample stage can often be heated or cooled to control the volatility of these by-products. Etches with strong chemical components are more isotropic, but introduce less damage to the semiconductor surface.

As with any other fabrication process, masks are needed to define the features to be etched. It is common that the etch used for the semiconductor also etches the masking material. For this reason, many different masks are used in etching, including photoresist, dielectric films, and metals. Masking can be a complex issue, especially when very deep etches ($>5\,\mu$m) are performed with high aspect ratios (170).

Gases for Etching. The primary factor in choosing a gas for dry etching of compound semiconductors is its ability to form volatile compounds with the semiconductor's constituent atoms. These volatile compounds are either thermally desorbed from the surface or desorb through an ion-assisted process (171). All gases used have a physical component associated with its ability to sputter the semiconductor surface. A wide variety of gases have been used in the etching of

compound semiconductors and listing them all is beyond the scope of this article. A short listing of gases for various semiconductors is shown in Table 5 (172,173).

6.3. Ion Implantation. Although a great number of compound semiconductor devices make use of epitaxy to form the core vertical structure of the device, ion implantation is a powerful tool in creating both horizontal and vertical modifications to a device. Ion implantation can be used to dope a semiconductor either n- or p-type by using appropriate species. Implantation can also be used to render a region semiinsulating or to initiate multilayer intermixing.

Ion Implantation Systems. An ion implantation system is used to accelerate ionized atomic or molecular species toward a target sample. The ionized species penetrates the surface of the sample with the resulting depth profile dependent on the implanted species mass, energy, and the sample target's tilt and rotation. An implanter's main components include an ionizer, mass separator, acceleration region, scanning system, and sample holder (190).

The implanted ion can be singly or multiply charged and can be any isotope. The mass separation system is used to avoid contamination. As an example, when implanting silicon the $^{29}Si^{+}$ isotope is often used instead of $^{28}Si^{+}$ to avoid contamination from the $^{28}N^{+}{}_{2}$ and $^{14}N^{2+}$ signals. After mass separation, the ions are electrostatically accelerated to their final energy, which can range from 5 keV to a few MeV. The deflector system and sample stage vary greatly system from system (191). Most implanters have some ability to tilt and rotate the sample with respect to the incoming beam. This is often used to avoid channeling of ions within the crystalline lattice of the semiconductor (192), achieving a more abrupt profile.

Implantation Basics. The depth distribution of the implanted species is a function of the acceleration energy, the ion mass, and the density and crystal structure of the sample (191). Two key parameters of the distribution are the projected range, ie, where the peak occurs, and the longitudinal straggle, which represents the spread of the implant. The implanted ion penetrates deeper into the sample for a higher implant energy, a lighter ion, or a less dense substrate. The depth distribution of the ions can be described by numerous analytical approximations including Gaussian and the more accurate Pearson IV models (191). The simpler Gaussian approximation has the following form, where $C(x)$

$$C(x) = \frac{D_0}{\Delta R_p \sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{x - R_p}{\Delta R_p}\right)^2\right]$$

is the ion concentration in cm^{-2}, R_p (cm) is the projected range, ΔR_p (cm) is the straggle, D_0 is the implanted dose in cm^{-2}, and x (cm) is the depth into the sample from the surface.

Many different materials can be used to spatially mask an implant on the semiconductor surface. Such masks include photoresist, dielectrics, and metals. In order to be an effective implant mask, the material should be thick enough to prevent the implant from penetrating the mask and entering the sample. A minimum thickness for stopping 99.99% of the ions in the masking material is (190).

When the implanted species enters the crystalline semiconductor it is slowed by a combination of electronic and nuclear scattering events (191). The nuclear scattering events leave significant lattice damage, including vacancies, interstitials, and antisite defects that must be repaired before the sample is useful. This is accomplished by thermal annealing. The high temperature anneals allow the lattice atoms to reintegrate into the crystalline lattice. At the same time, this annealing allows the implanted atoms to occupy lattice sites or become substitutional (193). This is often necessary for dopant atoms to become electrically active. If the implant is meant as an isolation step the annealing may be skipped as this might destroy the isolation. Treatment of the sample surface is critical during the anneal as the compound semiconductors often decompose at the high temperatures needed for activation. Samples are often annealed with a dielectric cap to prevent decomposition or are placed face down on a sacrificial sample to induce a local Group V over pressure (193). Rapid thermal annealing (RTA) has been replacing furnace annealing as the predominant annealing technique. This annealing has rapid rise and fall times during the temperature cycling that makes it easier to more consistently anneal samples with good activation and good surface control.

n- and p-Type Doping. Ion implantation can be an effective technique for the selective incorporation of dopant atoms in a device structure. Although not possessing the atomic level precision of epitaxy, ion implantation is capable of defining submicrometer features in both vertical and horizontal directions. A wide variety of dopants have been used to dope the compound semiconductors.

The most common n-type dopants for the III–V semiconductors include silicon, sulfur, selenium, and tellurium (193). Silicon is the most popular as it suffers very little from diffusion during the anneal step following implantation, and generally has activation percentages $>70\%$. In general, these dopants have good activation percentages except for high dose conditions. The heavier atoms (eg, tellurium) cause a great deal of lattice damage during implant, making it difficult to completely repair the lattice and causing a reduced activation percentage. Although silicon does not suffer from diffusion, it does suffer from amphoteric behavior. Being a Group IV element the silicon can occupy either the Group III or V lattice site. Proper annealing conditions, eg, excess Group V and/or capping materials, are useful in ensuring high donor concentrations of silicon (193). The maximum n-type doping level achievable is $\sim 2\text{–}4 \times 10^{18}\,\mathrm{cm}^{-3}$, which is lower than that for p-type doping (194).

For p-type doping in the III–Vs the most common dopants are beryllium, magnesium, zinc, carbon, and cadmium (193). The p-type dopants generally suffer from significant diffusion during the activation anneal (193). It is important to balance the anneal to achieve good activation without catastrophic diffusion. Beryllium generally displays excellent activation due to its light mass, which causes minimal lattice damage during implantation. Because the maximum acceptor concentration in the III–Vs is higher than that for donors, higher implantation doses can be used for p-type dopants. It is not unusual to achieve p-type dopant concentrations of $10^{20}\,\mathrm{cm}^{-3}$, although these samples often show serious diffusion. The diffusion of p-type dopants is often concentration dependent, getting worse with increasing concentration (195). Carbon is a p-type dopant that shows very little diffusion during annealing, but suffers from very

poor activation. Coimplantation is often required to get acceptable activation levels with carbon implantation (196).

Ion implantation has been successfully used to dope the III–Sb material system. Sulfur has been used as an n-type dopant, although with poor activation efficiencies (197). p-Type doping has been achieved using beryllium, zinc, and magnesium (197,198). Activation of the p-type dopants is generally much better, near 50%. For the Sb-containing materials the postimplant anneal is conducted at much lower temperatures, typically $< 600^{\circ}$C.

Because of the relative immaturity of the III–N material systems and the difficulties associated with growing high quality films, only a small amount of ion implantation work has been carried out in this material system, including work on the physical properties of range and diffusion (199), isolation (200,201), and n- and p-type doping of GaN (202). One of the reasons for the lack of success in ion implantation doping of GaN is due to the difficulty in activating the implanted species and repairing the lattice damage. Some success has been achieved at annealing at pressures of 1.6 GPa and temperatures of 1550°C (203), however, these materials are typically not as good as samples doping during MOCVD growth. Unlike the abundant work on ion implantation into the III–Vs, this technique has not been extensively used in the II–VI compound semiconductors. However, there are reports of work being done in doping HgCdTe (204) and other II–VI materials (205).

Isolation. Besides making semiconductor samples conducting, the other main use of ion implantation is to cause a region to be semi-insulating. This can be accomplished by two techniques: lattice damage or chemical modification. The damage caused by an implanted ion can cause a sample to become semiinsulating for the proper implant dose and energy. This is a temporary condition that can be reversed by thermal annealing (206). Typical ions that are used in this technique include hydrogen and oxygen. For very narrow band gap materials it is difficult to form good isolation regions due to thermal carrier generation.

To provide a more permanent isolation region an ion must be implanted that causes the sample to be semi-insulating after annealing. The most common ion used is oxygen (206), although iron has also been used in InP. Oxygen forms chemical compounds, which are deep trap states in compound semiconductors, depleting the samples of mobile charge. Deep trap states do not form in all semiconductors.

Intermixing. In some fabrication sequences it is desirable to cause the interdiffusion of semiconductor superlattices. This effect causes a distinct two-material superlattice to interdiffuse, transforming into a single nearly homogeneous material. The optical and electrical properties of the new material is different from that of the superlattice. Extensive work has been done in the GaAs–AlGaAs material system using both silicon implantation (207) and proton implantation (208). Some work has also been carried out in other material systems such as InP–InGaAs (209,210) and InAlAs–InP (211).

6.4. Metallization. Metals can be used in compound semiconductor processing for the formation of ohmic contacts, Schottky contacts, and interlevel wiring. There are vastly different requirements for each of these applications that has resulted in a large variety of metals being used in fabrication technologies. Good ohmic contacts should have low contact resistivity and good thermal

stability. Good Schottky contacts should have clean interfaces with good barrier heights and thermal stability. Interlevel wiring should have low resistances with good adhesion.

Metal Deposition Systems. Metals can be deposited by a variety of techniques including thermal evaporation, electron beam evaporation, sputtering, and CVD. The most common of these techniques include thermal and electron beam evaporation. Both systems are identical except for the method used to heat the metal target. In each system, the semiconductor sample and the metal target are located within a vacuum chamber that can be evacuated out to $<1.3 \times 10^{-4}$ Pa (1×10^{-6} Torr). The semiconductor sample surface is facing the metal target at a distance of usually 30 cm or more. There is a shutter between the metal target and the semiconductor to rapidly begin and end the deposition. The metal target is heated by one of two techniques: resistive or electron beam heating. The metal is evaporated from the target and deposited on the semiconductor surface. The amount of material deposited is monitored by a crystal oscillator. A common form of masking for evaporation is called lift-off (172). The masking material, often photoresist, is defined with a reentrant profile that causes a break in the metal deposited on the semiconductor surface and the metal deposited on the masking surface. After metal deposition the masking material is chemically dissolved, lifting off the excess metal on the mask, leaving clearly defined metal regions on the semiconductor surface. Common metals used in thermal or electron beam evaporation include gold, titanium, platinum, palladium, nickel, germanium, and chrome.

Another common technique for metal deposition is sputtering (212). Sputtering is used for metals with high melting points that cannot easily be deposited by evaporation techniques or in situations where good step coverage is required. Additionally, reaction sputtering can also be used to form metal compounds such as TiN, by sputtering titanium in a nitrogen ambient (212). In a sputtering system, a plasma is used to physically sputter the metal from a target that is then deposited on the semiconductor surface. Common metals for sputtering include tungsten, tungsten–silicide, titanium, tantalum, and transparent conductors, eg, indium tin oxide (ITO). Sputtering has a more isotropic deposition, making it difficult to use the lift-off technique. It is more common to employ postdeposition dry etching to define the metal.

The last technique commonly employed to deposit metals for compound semiconductors is electroplating (172). This technique is usually used where very thick metal layers are desired for very low resistance interconnects or for thick wire bond pads. Another common use of this technique is in the formation of air-bridged interconnects (172), which are popular for high speed electronic and optoelectronic circuits.

Metals for Ohmic Contacts. The main goal of an ohmic contact is to provide a low resistance contact to a heavily doped semiconductor region. Depending on the semiconductor to be contacted, the doping level, and the desired application, there are a number of different metallization schemes that can be used. In general, it is easiest to make good ohmic contacts to heavily doped narrow band gap semiconductors. Additionally, as the alloy composition and band gap of a ternary of quaternary semiconductor changes, so does the quality of an ohmic contact made to the alloy. The most common form of contact used is the alloyed

contact. Following metal deposition the contact and semiconductor are annealed to allow intermixing of the metal–semiconductor interface (213). This mixing introduces components of the metal into the semiconductor, often doping it to provide a low contact resistance contact. Table 6 lists a variety of contact metals, including a number of alloyed systems. An excellent list of alloyed contacts for GaAs is available (214).

Many different metals have been used for a variety of semiconductors, and Table 6 lists only a small number of the possible combinations. The alloyed contact is not very shallow, because of mixing, and often has poor thermal stability because of continued interaction of the metals (213). Another approach is the nonalloyed contact, which displays ohmic behavior after deposition, requiring no further thermal processing. Unfortunately, this scheme cannot be used at all times. In general nonalloyed contacts require very high doping levels ($>10^{19}\,cm^{-3}$) and/or low band gap semiconductors.

A third technique for ohmic contact formation is solid-phase regrowth (SPR) (213). The SPR contact involves a modification of the deposited metals during thermal processing. The overall concept is that a thin epitaxial layer of the metal (usually Ge or Si) forms on the GaAs surface, providing a low resistance contact (213). The SPR contact is very shallow and can have good thermal stability. Although the SPR contact involves some postdeposition thermal processing, it does not suffer from the same metal–semiconductor mixing of the alloyed contact. Table 6 lists a number of SPR contacting recipes that have been successfully developed for compound semiconductors. One last technique involves the use of refractory metals in the ohmic contact. These contacts are useful for high temperature applications, where the refractory metals do not melt or mix with the semiconductor. Although the contact resistances for these contacts are not as good as alloyed contacts, the improved thermal stability can be more important for specific applications.

Metals for Schottky Contacts. Good Schottky contacts on semiconductor surfaces should not have any interaction with the semiconductor as is common in ohmic contacts. Schottky contacts have clean, abrupt metal–semiconductor interfaces that present rectifying contacts to electron or hole conduction. Schottky contacts are usually not intentionally annealed, although in some circumstances the contacts need to be able to withstand high temperature processing and maintain good Schottky behavior.

The most common Schottky contacts for compound semiconductors are gold-based metallizations deposited by thermal or electron beam evaporation. The metal may include a thin titanium layer in direct contact with the semiconductor that acts as an adhesion layer. Additionally, a thin layer of a diffusion barrier metal, such as platinum, can be placed between the titanium and the gold. Table 7 lists some standard Schottky contacts used for compound semiconductors. One problem with gold-based Schottky contacts are their poor thermal stability and inability to withstand high processing temperatures. The lift-off technique is often used in defining gold-based Schottky contacts.

A popular alternative to gold-based Schottky contacts is the use of refractory-based metals, eg, tungsten, tungsten silicide, or titanium nitride. These metals are deposited by sputtering and usually require postdeposition etching to define the contact region. These contacts usually have much better

thermal stability and are often used in processes when high temperature anneals ($>800^{\circ}C$) are used after contact formation. One drawback of using refractory metals is the high resistance of the metal as compared to gold-based contacts. This resistance can have deleterious effects on device performance.

Metals for Interlevel Wiring. The most common metals for interlevel wiring on compound semiconductors are gold, titanium–gold, and aluminum. The metals are used to connect individual devices into circuits. The metals are often required to travel over interlayer dielectric films, making contact to both Schottky and ohmic contact regions. The interlevel wiring should have low resistance for thin wires and should not suffer from any reactions with dielectrics, metals, or the semiconductor. Although aluminum is cheap and widely used in silicon processing it is not often used in high speed compound semiconductor circuits due to its resistance and known stability problems (190). Gold-based wiring is more common because of its excellent conductance and nonreactivity.

6.5. Dielectric Overlayers. Unlike silicon processing, where metal oxide semiconductor (MOS) devices are a crucial technology, dielectric films in compound semiconductor processing have generally played a secondary role. There has been a great deal of research in trying to develop metal insulator semiconductor (MIS) devices for compound semiconductors, but successes have been fairly limited. A more common use of dielectric insulators is in encapsulation, planarization, interlevel dielectric spacers, and surface protection during annealing.

Dielectric Deposition Systems. The most common techniques used for dielectric deposition include CVD, sputtering, and spin-on films. In a CVD system, thermal or plasma energy is used to decompose source molecules on the semiconductor surface (212). In plasma-enhanced CVD (PECVD), typical source gases include silane, SiH_4, and nitrous oxide, N_2O, for deposition of silicon nitride. The most common CVD films used are silicon dioxide, silicon nitride, and silicon oxynitrides.

Insulator sputtering is similar to the process described for metal sputtering. The only difference is that the source target is a dielectric film. There is less control of the chemical nature and quality of the film as compared to a CVD deposited film. Common sputtered films include silicon nitride and silicon oxide.

A number of dielectric films are deposited by the spin-on technique. In this case, the film's constituent molecules are dissolved in a solvent to form a liquid. After spinning the liquid over a semiconductor surface the solvent is driven off with a baking step, leaving behind the thin dielectric film. Common films include polyimide and benzocyclobutene (BCB). The deposition process for these films is simple, making it attractive for a manufacturing process.

Dielectrics for Metal Insulator Semiconductor Structures. The biggest problem in using dielectric films for MIS applications is the poor quality of the interface between insulator and semiconductor. Typically, this interface is characterized by a high density of traps that prevents good modulation of the carrier density in the semiconductor. The primary cause of these traps is a large density of dangling bonds on the semiconductor surface. In order to fabricate a high quality MIS structure, passivation of these dangling bonds is necessary. Some of the most common techniques for this include the use of sulfur passivation, either by

aqueous or plasma techniques (236). Sufficient progress has been made in the development of MIS structures that basic MISFETs are being fabricated in InP, GaAs, and InGaAs (236,237). Some attempts have also been made in using AlN as an insulator layer for GaAs-based MIS devices (238).

Dielectrics for Interlevel Wiring and Planarization. When connecting a number of devices to form a circuit it is often necessary to cross wires without actual electrical contact between them. In order to accomplish this, multiple levels of wiring separated by dielectric films are necessary. In some cases, it is possible to form bridges of metal using air as the dielectric (172). However, if more than two levels of wiring are required then dielectric spacing is necessary. The ideal dielectric film has excellent adhesion and a low dielectric constant to minimize parasitic capacitances. The most common films include silicon oxide, silicon nitride, and a number of spin-on dielectrics (239).

During the fabrication process the surface of the semiconductor is etched and metal contacts are deposited. These features can represent a topographical challenge to subsequent metal wiring levels. For this reason, it is important that the dielectric film used tends to smooth out such discontinuities as metal and etched edges (172,240). Additional applications for spin-on dielectrics include forming integrated microlenses for optoelectronics (241).

6.6. Lithography. There are a number of different techniques for pattern definition on a semiconductor sample, however, none are particular to compound semiconductors. The main goal of lithography is to accurately define a region to be modified, either by deposition, etching, or masking of an implant. The region to be modified is often defined by its location to previous features and therefore the accurate alignment of a mask to previous features is a significant component of lithography.

The most common method for the definition of a pattern is optical lithography. Optically sensitive resists are exposed to light that affects their dissolution rate when exposed to a developing solution. Resists that etch away when exposed to uv light are referred to as positive tone, whereas resists that become etch resistant when exposed to light are referred to as negative tone. In general, positive tone resists provide higher resolution and are more useful in a number of fabrication steps. Techniques for masking the resist include contact printing and projection printing (172). In contact printing, a glass plate with a patterned metal mask is put in contact with the resist-coated sample and light is shown through the mask. In a projection system, the mask is held a fixed distance from the sample and light is focused through the mask and onto the sample. Projection systems can include pattern reduction optics after the mask. Typically, these systems employ stepping of the semiconductor wafer, exposing a single die at a time. Both techniques are in use, with stepper projection systems more popular in production facilities. The resolution of optical techniques is basically limited by the wavelength of the light used to expose the mask. Modern optical systems accurately define features of 0.25-μm resolution, and are getting smaller annually.

To achieve smaller dimensions, there are systems that use X-rays instead of optical photons (172). These systems require a collimated X-ray source that is often expensive. Additionally, systems have been developed that use ion

beams to expose the resist. Either an X-ray or ion beam system requires specialized resists and exposure systems.

A maskless lithographic technique commonly referred to as *e*-beam lithography, uses high energy steerable electron beams (172). These systems operate with very narrow beams of electrons having energies ranging from 25 to 100 keV, depending on the particular system. The electron beam is electrostatically scanned around the sample surface, exposing the resist to the electrons. The electrons can cause the resist to either cross-link or break down depending on the exact chemistry of the resist. The noncross-linked resist is then etched away in a development process. Typical electron beam lithography systems can achieve minimum feature dimensions. They are popular in the production of masks for both optical and X-ray techniques as well as for direct writing on semiconductor surfaces. However, the low throughput of *e*-beam systems makes them presently intractable for production use in most circumstances. They are particularly popular in research laboratories exploring nanoscale ($< 0.1\,\mu m$) devices.

7. Acknowledgment

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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Table 1. **Physical Properties of Some Compound Semiconductors**

Compound	Band gap, eV	I or D[a]	Crystal symmetry[b]	Lattice constants a, c Å[c]	$T\,\Delta a(T)$, $\Delta c(T) \times 10^6\ \mathrm{K}^{-1}$[d]	Bulk modulus, GPa[e]	Melting temperature, °C[f]	Typical MOCVD growth T, °C[g]
				IV–IV				
SiC (6H)	2.996	I	w	3.086, 15.117	4.3, 4.7	221	2830	>1500
				III–V				
InSb	0.18	D	z	6.4794	5.37	47	525	<520
InAs	0.354	D	z	6.0584	4.52	60	942	420–490
InP	1.344	D	z	5.8697	4.60	71	1062	600–650
InN	0.7–1.4	D	w	3.53, 5.69	3.8, 2.9	140	1100	600–800
GaSb	0.75	D	z	6.0959	7.75	57	712	<550
GaAs	1.424	D	z	5.6533	5.73	75	1238	600–700
GaP	2.26	I	z	5.4505	4.65	89	1457	800
GaN	3.4	D	w	3.189, 5.186	3.17, 5.59	195	2220	1050
AlSb	1.686	I	z	6.1355	4.5	58	1065	720–820
AlAs	2.168	I	z	5.6611	5.0	77	1750	600–800
AlP	2.505	I	z	5.4672	3.5	86	2550	>760
AlN	6.2	D	w	3.112, 4.982	4.15	202	3000	>1100
BP	2.1	I	z	4.54	4.0	172	1125	600–1000
BN	5.4–7.0	I	z	3.615	3.5	358	2966	700–1200

Table 1. (*Continued*)

Compound	Band gap, eV	I or D[a]	Crystal symmetry[b]	Lattice constants a, c Å[c]	$T\,\Delta a(T)$, $\Delta c(T) \times 10^6\ K^{-1}$[d]	Bulk modulus, GPa[e]	Melting temperature, °C[f]	Typical MOCVD growth T, °C[g]
				II–VI				
ZnO	3.35	D	w	3.252, 5.313	2.9, 4.75	144	1974	~450
ZnS	3.68	D	w	3.82, 6.26	4.59, 6.54	77	1700	350
ZnSe	2.71	D	z	5.671	7.2	62	>1100	450–620
ZnTe	2.25	D	z	6.1037	9.3	51	1239	300–440
CdS	2.42	D	w	4.16, 6.756	2.77, 4.30	62	1240	300–500
CdSe	1.73	D	w	4.299, 7.010	2.76, 4.13	53	1240	300–500
CdTe	1.56	D	z	6.481	4.96	42	1240	350–380
HgTe	−.303	M	z	6.401	5.2	42	670	250–370

[a]The electronic transitions are either direct (D) or indirect (I).
[b]The crystal symmetry is either wurtzite (w) or zinc blende (z) which also known as cubic.
[c]Two constants (a and c) are needed to describe the wurtzite lattice and only one constant (c) is needed to describe the zinc blende lattice.
[d]The linear thermal expansion coefficients. One parameter is required for zinc blende and two are required for wurtzite.
[e]The bulk modulus given in GPa.
[f]The melting temperature in °C.
[g]Typical MOCVD growth temperature given in °C.

Table 2. **Transport Properties[a] of Some Zinc Blende Binary Compound Semiconductors**

Compound	E_Γ, eV[b]	E_L, eV	E_X, eV	Δ_0, eV	m_Γ	γ_1[c]	γ_2[c]	γ_3[c]	m_{lh}[d]	m_{hh}[d]
					III–V					
InSb	**0.18**	1.35	1.78	0.803	0.014	33.2	14.8	15.5	0.016	0.362
InAs	**0.35**	1.55	1.90	0.371	0.023	20.4	8.30	9.10	0.026	0.352
InP	**1.34**	2.03	2.38	0.108	0.079	4.59	1.65	2.35	0.11	1.238
GaSb	**0.75**	0.80	1.03	0.764	0.041	13.30	4.20	5.50	0.043	0.299
GaAs	**1.42**	1.74	1.90	0.341	0.067	6.85	2.10	2.90	0.083	0.592
GaP	2.78	2.64	**2.26**	0.085	0.172	4.04	0.53	1.26	0.167	0.475
AlSb	2.30	2.21	**1.69**	0.673	0.12	4.69	1.24	1.62	0.131	0.570
AlAs	3.03	2.36	**2.19**	0.302	0.146	3.46	0.88	1.26	0.176	0.804
AlP	3.60		**2.51**	(0.053)	(0.169)	(3.00)	(0.63)	(1.15)	(0.205)	(0.896)
					II–IV					
ZnS	**3.68**				(0.295)	(2.31)	(0.34)	(0.65)	(0.309)	(0.724)
ZnSe	**2.71**				0.165	3.0	0.53	0.92	0.229	0.614
ZnTe	**2.25**				0.13	3.9	0.83	1.30	0.168	0.536
CdTe	**1.56**				0.096	4.11	1.08	1.95	0.144	0.797
HgTe[e]	**−0.30**				−0.033	−15.6	−9.6	−11.2	−0.028	0.205

[a]Values in parentheses are estimates.

[b]Band-gap energies at three symmetry points. The minimum band-gap energy is in bold. If the minimum occurs at E_Γ the bandgap transition is direct (D) while if the minimum is at E_L or E_X the bandgap transition is indirect (I).

[c]Luttinger parameters.

[d]The light (l) and heavy (h) hole masses are the spherical average values defined in text.

[e]The negative electron and light hole masses listed for HgTe are a consequence of its being a semimetal rather than semiconductor. The curvatures of these two bands are inverted with respect to the convention defined for semiconductors.

Table 3. **Optical and Transport Properties[a] of Some Compound Semiconductors**

Compound	ϵ_0[b]	n_∞[c]	Breakdown field, $\times 10^4$ V/cm	Peak velocity $\times 10^6$ cm/s	$\mu_{e\ 300K}$[d], cm^2/Vs	$\mu_{h\ 300K}$[e], cm^2/Vs	n-Type dopants	p-Type dopants
				IV–IV				
SiC (4H)	9.77	2.55	300–500	≤8.0	≤900	≤120	N, Cr	Al, Ga
				III–V				
InSb	16.8	4.0	0.1	70	77, 000	≤850	Te, Sn	Cd
InAs	15.5	3.51	4		33, 000	450		
InP	12.5	3.1	50	40	4600	150	Si, Ge	C, Zn
InN	(15.3)	(2.9)	1.2	43	3200		Si, Ge	
GaSb	15.7	3.8	5	6	≤3000	≤1000	Te, Se	Zn, Ge
GaAs	12.9	3.3	6	22	8500	400	S, Si	C, Zn
GaP	11.1	3.02	100	12	110	75	S, Si	C, Zn
GaN	8.9	2.3	> 500	31	1500	30	Si, Ge	Mg, Zn
AlSb	12.4	3.3		7	< 350	< 400		
AlAs	10.9	3.0		6	200	100		
AlP	9.8				60	450		
AlN	8.5	2.1	(≤140)	17	(300)	(14)	Si	Mg, Zn
BP	9.95	2.7						
BN	7.1	2.12	(≤600)		(< 200)	(< 500)	S	Be
				II–VI				
ZnO	8.66	2.0	(> 100)	30	200	(< 20)	Al, Ga	N
ZnS	8.9	2.39		20	130	<		
ZnSe	7.6	2.32			< 600		Cl	Li, N
ZnTe	7.28	3.18			< 650	100		
CdS	8.5	2.5			300			
CdSe	8.41				500			
CdTe	7.4	3.19			(1000)			
HgTe	21.0	3.90			–			

[a]Values in parentheses are estimates.
[b]static dielectric constant.
[c]refractive index.
[d]Electron mobility.
[e]Hole mobility.

Table 4. **Wet Etches for Compound Semiconductors**

Semiconductor	Etch	Typical rates, μm/min	References
GaAs	H_3PO_4:H_2O_2:H_2O	0.01–4.0	159
[a]	$C_6H_8O_7$:H_2O_2	0–0.3	155
[b]	H_2SO_4:H_2O_2:H_2O	3–14	159,160
[c]	NH_4OH:H_2O_2	0.1	161
AlGaAs	$C_6H_8O_7$:H_2O_2	0–0.2	155
InGaAs	$C_6H_8O_7$:H_2O_2	0–0.14	155
InP	HCl	6	162
	HCl:H_3PO_4	0.1–1.0	163
	Br–CH_3OH	0.4	162
InAs	$C_6H_8O_7$:H_2O_2	0.09	164
InSb	I_2:CH_3OH		165
GaSb	HNO_3:HF:CH_3COOH		165
[d]	$C_6H_8O_7$:H_2O_2	0.9	164
CdTe	Br:CH_2OHCH_2OH	0.08	166
ZnTe	HNO_3:HF		165
ZnS	$K_2Cr_2O_7$:H_2SO_4		165
AlN[e]	photoresist developer	0.01–1	167
GaN[d]	NaOH–H_2O	2	168
InN[d]	HCl–HNO_3	1	168

[a] GaAs selective to AlGaAs.
[b] GaAs at 300 K.
[c] GaAs agitated.
[d] Rate = nm/min.
[e] Active component is KOH.

Table 5. **Dry-Etch Gases for Compound Semiconductors**

Semiconductor	Etch method (gas)[a]	References
GaAs, AlGaAs	RIE ($SiCl_4$ or Cl_2)	174
	RIE (CH_4–H_2)	175
	ECR (CH_4–H_2–Ar)	176
	ECR (HBr)	177
	ECR (CCl_2F_2, $SiCl_4$, or BCl_3)	178
	ion milling (Ar)	169
InP	RIE (CH_4–H_2)	179
	RIE (Cl_2–H_2)	180
	ECR (CH_4–H_2–Ar)	181
	ECR (Cl_2–H_2)	182
	ECR (HBr)	177
	ion milling (Ar)	169
InGaAs, InAlAs	ECR (HBr or CH_4–H_2)	177,183
GaSb	RIE (Cl_2 or $SiCl_4$)	174
	hybrid ECR (CCl_2F_2–O_2 or PCl_2)	184
GaN, InN, AlN	ECR (Cl_2H_2, BCl_3, or CCl_2F_2)	185,186
	ECR (HI–H_2–Ar or HBr–H_2–Ar)	187
HgCdTe, ZnS, CdTe	ECR (CH_4–H_2 or H_2–Ar)	188,189

[a]RIE = reactive ion etching; ECR = electron cyclotron resonance etching.

Table 6. **Ohmic Contacts for Compound Semiconductors**

Semiconductor doping, n or p	Metal system	Contact type[a]	Anneal temp, °C	Typical ρ_c,[b] $\Omega \cdot cm^2$	References
n-GaAs	Au–Ni–Ge	A	400	10^{-6}	215
	Ni–Ge–Au–W	A	650	1.3×10^{-6}	216
	Pd–Ge	SPR	250	1.5×10^{-6}	217
p-GaAs	Be–Au	A	525	1.2×10^{-7}	218
	Pd–Zn–Pd–Au	A	500	1×10^{-7}	219
n-InP	Au–Sn	A	400	2×10^{-6}	220
p-InP	Ge–Pd(Zn)	SPR	400	10^{-5}	221
p-InAs	Pt–Ti	NA		7.5×10^{-6}	222
n-GaN	Ti–Al	A	900	8×10^{-6}	223
	Au	A	575	10^{-7}	224
n-InN	Ti–Pt–Au	NA		2×10^{-7}	225
n-GaSb	Au–Te	A	400	10^{-6}	226
p-GaSb	Au–Zn–Au	A	300	10^{-6}	227
p-HgCdTe	Au	A	200	5×10^{-6}	228
p-ZnTe	Au–Pt–Ti–Ni	A	300	10^{-6}	229

[a]The contact type is alloyed, A; nonalloyed, NA; or solid-phase regrowth, SPR.
[b]Typical contact resistivity.

Table 7. **Schottky Barrier Heights for Metals on Compound Semiconductors**

Semiconductor	Metal	Barrier height, eV	References
n-GaAs	Au	0.90	214
	W	0.65	214
p-GaAs	Au	0.42	64
n-InP	Au	0.52	64
p-InP	Au	0.76	64
p-InAs	Au	0.47	64
p-CdMnTe	Al	0.73	230
n-GaN	Au	0.91	231
	Ti	0.58	232
n-InSb	Au	0.05	233
n-GaSb	Al	0.65	234
p-AlSb	Au	0.71	235

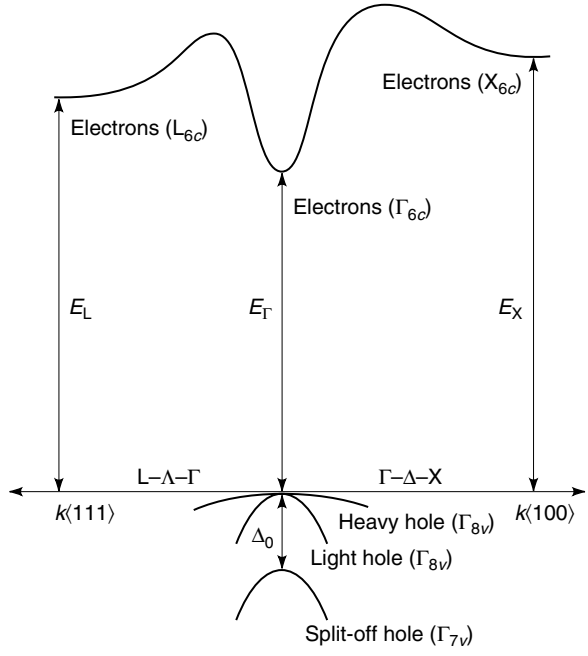

Fig. 1. Representation of the band structure of GaAs, a prototypical direct band gap semiconductor. Electron energy, E, is usually measured in electron volts relative to the valence, v, band maximum that is used as the zero reference. Crystal momentum, k, is in the first Brillouin zone in units of $2\pi/a$ where a is the lattice constant. In semiconductors with an indirect band gap the ordering of the valence (hole) states is unchanged, whereas the ordering of the conduction, c, states is inverted to $X < L < \Gamma$. In the semimetal HgTe the conduction band lies between the Γ_{8v} and Γ_{7v} valence bands and the curvatures of the Γ_{8v} light hole band and the Γ_{6c} electron band are inverted with respect to those shown for GaAs. The parameter Δ represents the line of symmetry.

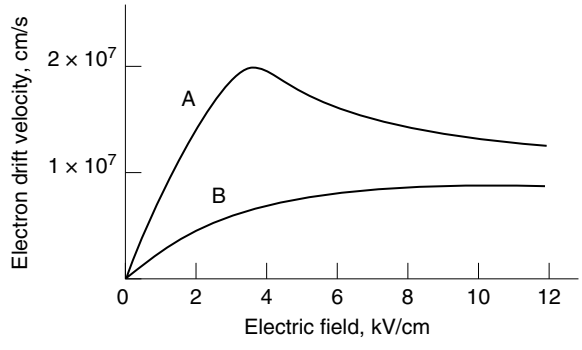

Fig. 2. Electron drift velocities as a function of electric field for A, GaAs and B, Si. The gradual saturation of curve B is characteristic of all indirect semiconductors. Curve A is characteristic of direct gap semiconductors and at low electric fields this curve has a steeper slope which reflects the larger electron mobility. The peak in curve A is the point at which a substantial fraction of the electrons have gained sufficient energy to populate the indirect L minimum which has a much larger electron-effective mass than the Γ minimum. Above 30 kV/cm (not shown) the drift velocity in Si exceeds that in GaAs.

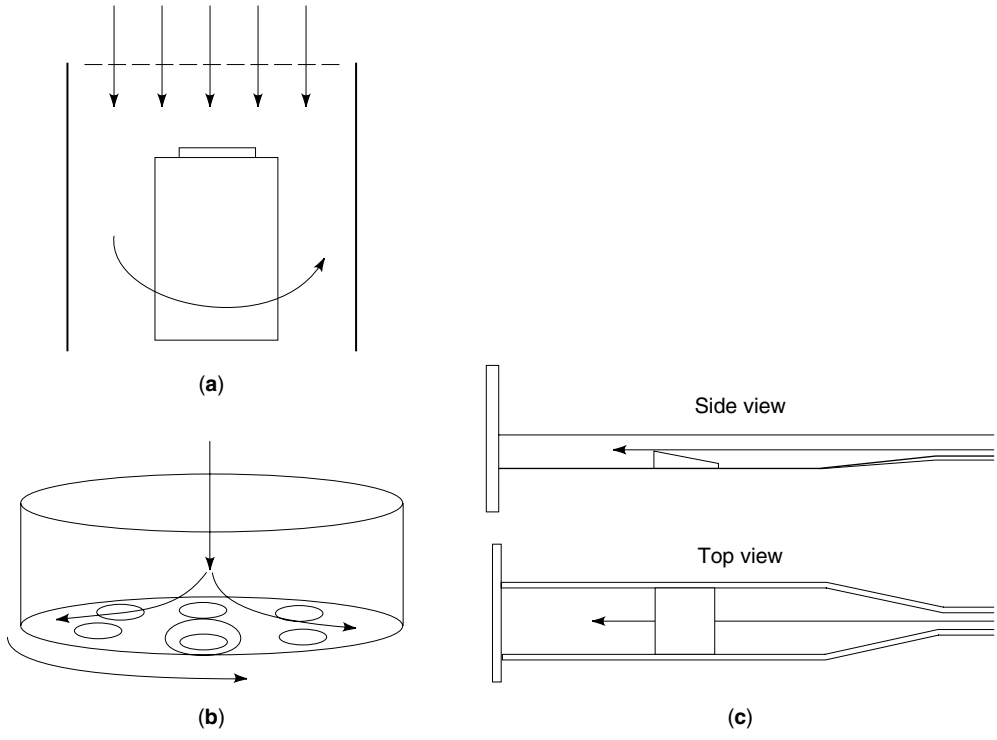

Fig. 3. Schematic of three commonly used types of MOCVD reactors where the arrows indicate gas flow: (**a**) vertical rotating disk where (– – –) represents an inlet to promote a laterally uniform gas flow, (**b**) planetary rotation, and (**c**) horizontal.

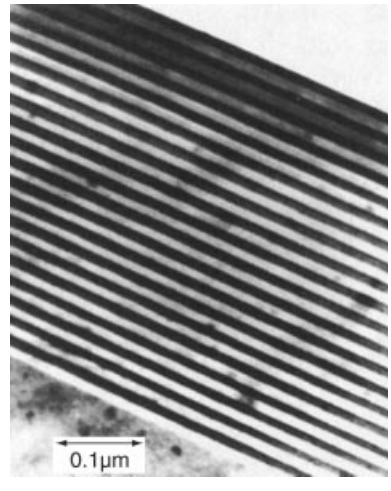

Fig. 4. A transmission electron photomicrograph of an InAsSb–InSb superlattice grown by MOCVD.

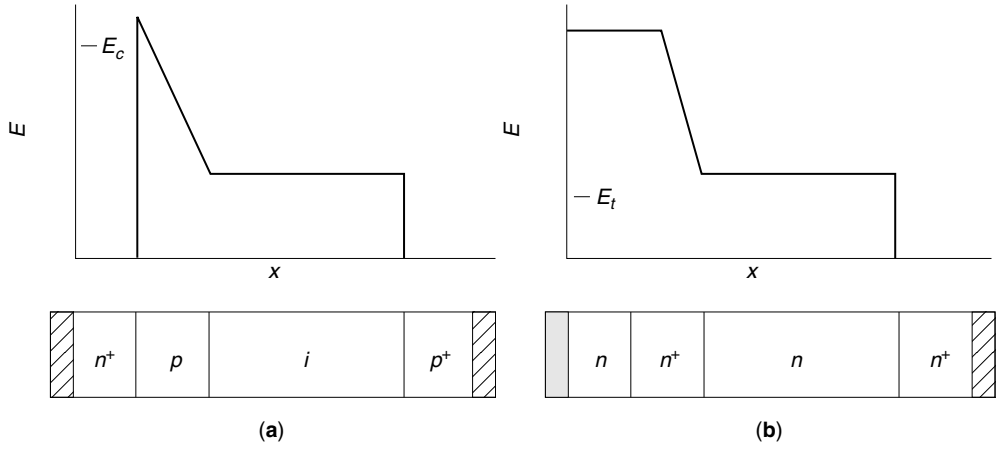

Fig. 5. Structures and electric fields for (**a**) Read IMPATT diode and (**b**) Schottky cathode TED, where ▨ represents ohmic and ■ Schottky contact, and *i* denotes the intrinsic or undoped region of the semiconductors.

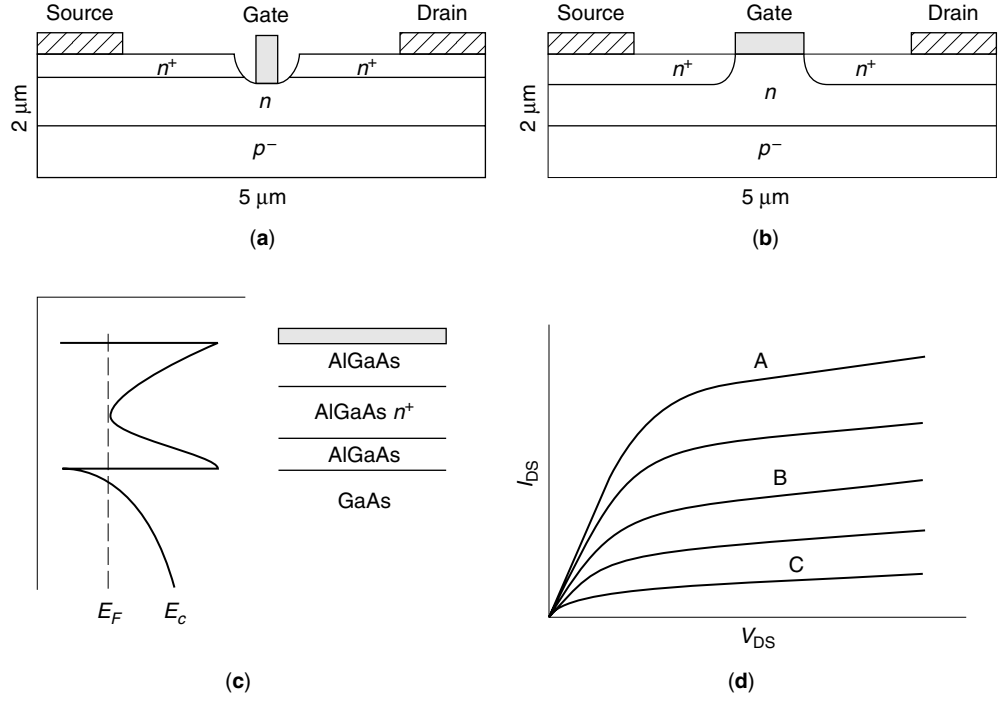

Fig. 6. (**a**) Recess gate FET geometry and (**b**) self-aligned FET geometry where ▨ represents ohmic and ■ Schottky contact; (**c**) layer structure and conduction band profile for a typical heterojunction FET (HFET), where E_c is conduction band edge energy and E_F is Fermi energy; and (**d**) typical I–V characteristics for a d-mode FET, where I_{DS} is the source-to-drain current, V_{DS} is source-to-drain voltage, and gate voltage, V_g, for A is >0; B, $V_g = 0$; and C, $V_g < 0$.

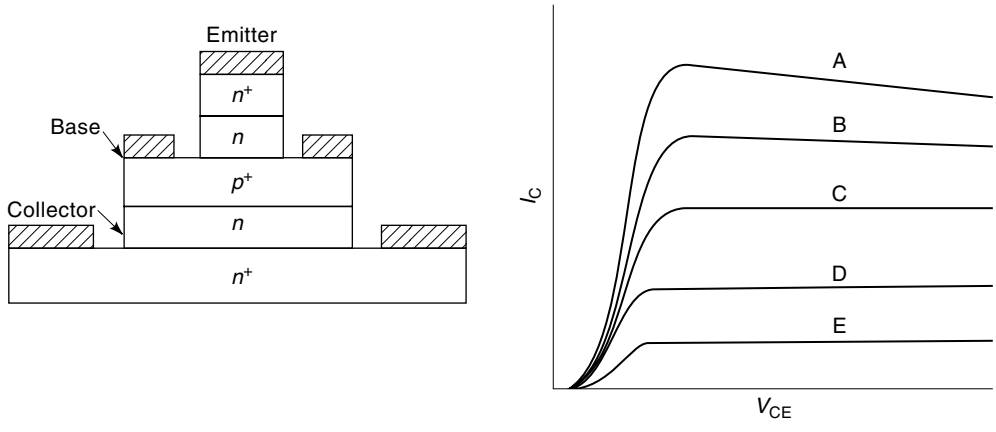

Fig. 7. (**a**) Generic structure of an emitter-up HBT and (**b**) typical I–V characteristics of an HBT, where A shows I_{B5}; B, I_{B4}; C, I_{B3}; D, I_{B2}; and E, I_{B1}.

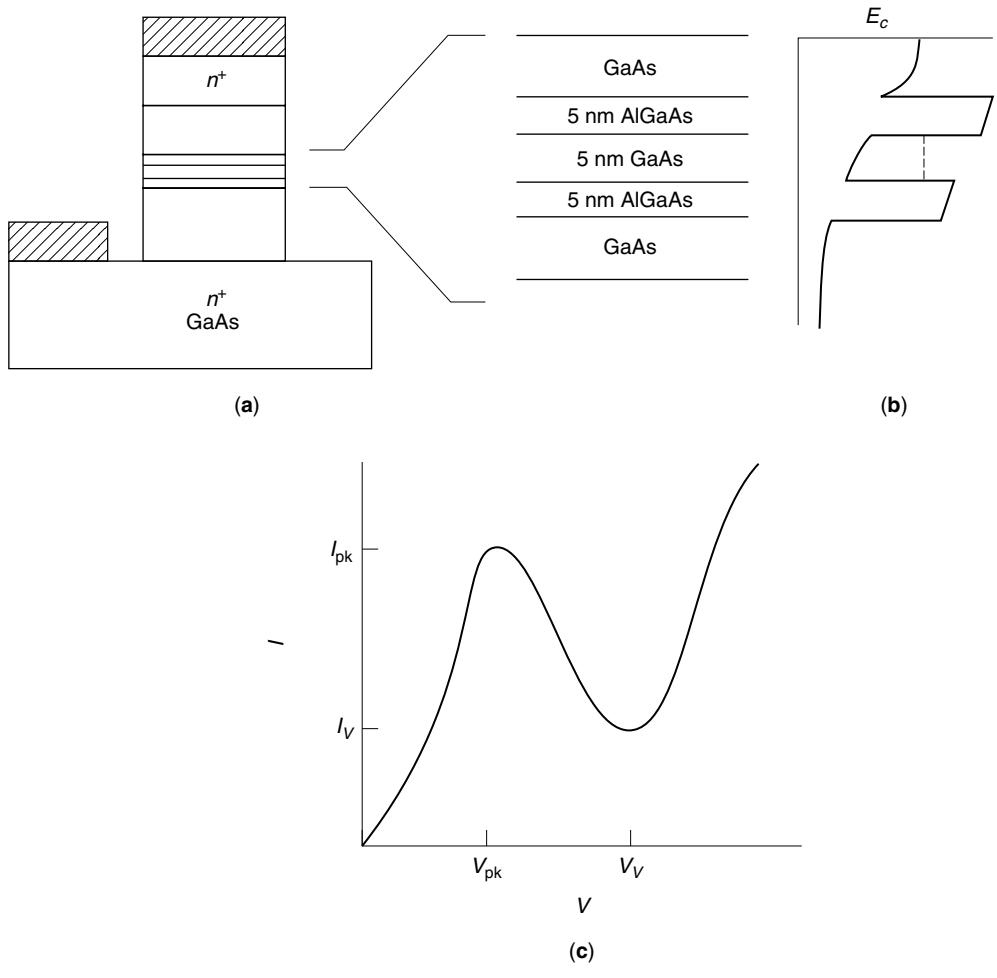

Fig. 8. (**a**) Structure of a typical resonant tunneling diode (RTD); (**b**) conduction band diagram for the barrier structure where (–) represents the resonant state; and (**c**) typical I–V characteristics for a RTD.

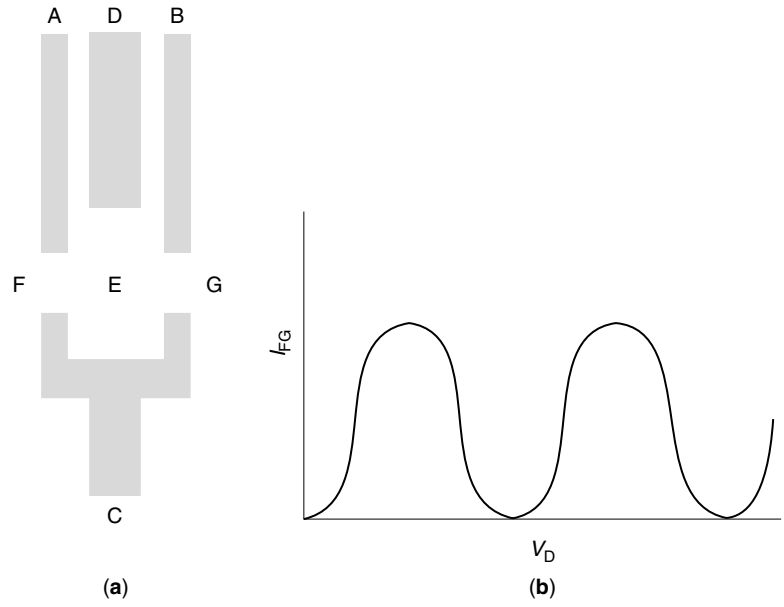

Fig. 9. (**a**) Top view of a Coulomb blockade device (single-electron transistor) patterned on an AlGaAs–GaAs heterojunction, where ■ = the surface gate; (**b**) I–V characteristics for a Coulomb blockade device.

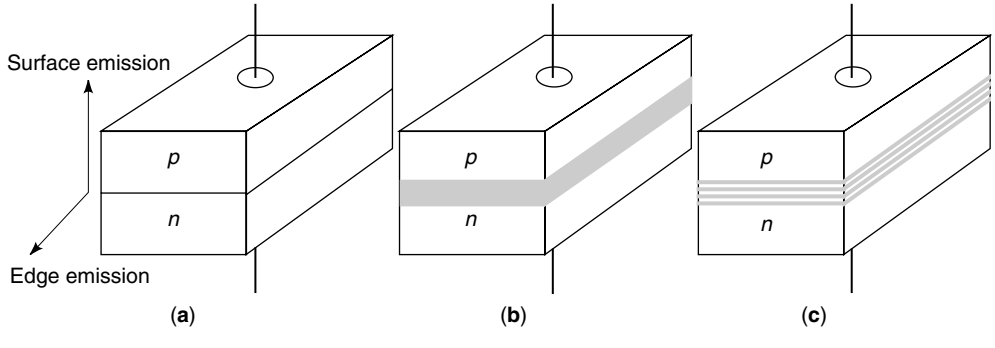

Fig. 10. Schematic of various LED and laser diode structures where ■ signifies material of a lower energy band gap: (**a**) homojunction, (**b**) double-heterojunction (DH), and (**c**) multiquantum well (MQW) structures.

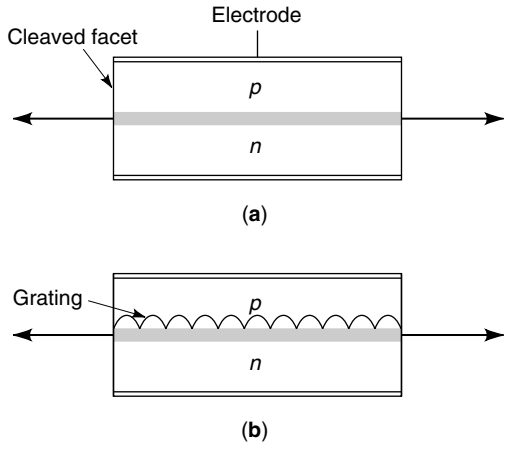

Fig. 11. Schematic of edge-emitting laser diodes where the arrows represent the direction of laser emission and ■ represents the active region: (**a**) standard structure with cleaved facets for mirrors and (**b**) distributed feedback (DFB) laser that employs coherent reflection from a grating to generate optical feedback.

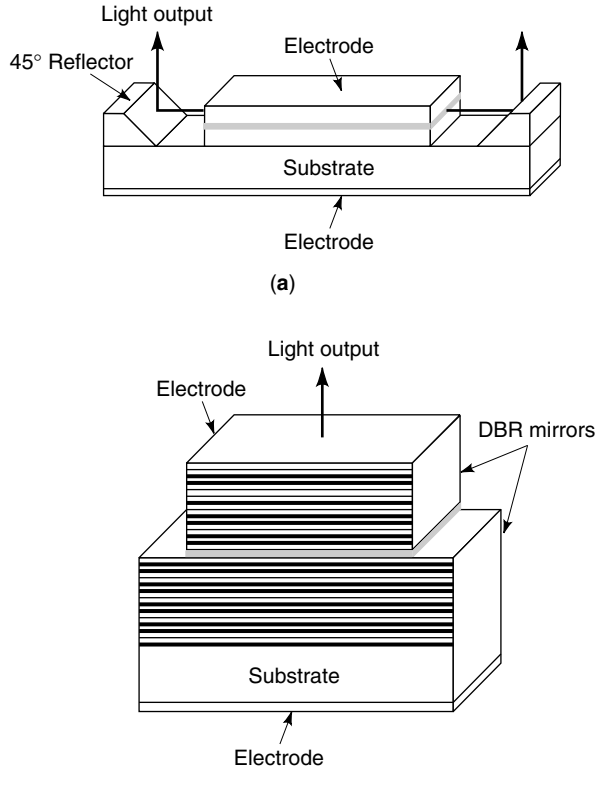

Fig. 12. Schematic of surface-emitting laser diodes where ■ represents the active region: (**a**) planar cavity surface-emitting laser diode (PCSEL) with 45° etched reflectors and (**b**) vertical cavity surface-emitting laser diode (VCSEL) with semiconductor-based multilayer mirror stacks grown into the structure. DBR = distributed Bragg reflector.

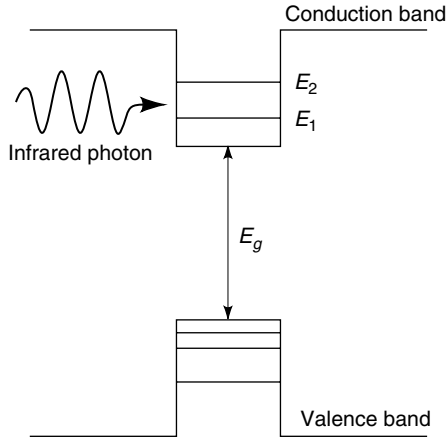

Fig. 13. Absorption between confined energy levels in a quantum well ir photodetector (QWIP). The energy difference (E_2–E_1) between the confined energy levels in a quantum well may be designed such that it is resonant with ir radiation. The band gap, E_g, is much greater, therefore direct band gap absorption does not occur.